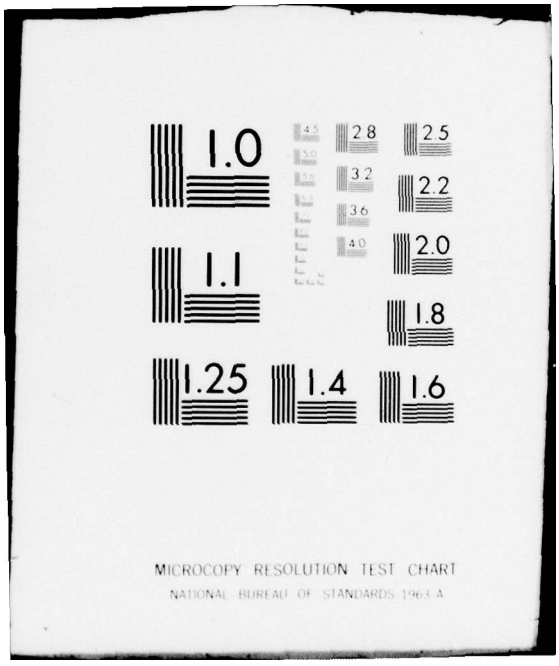
AD-A073 350 AERONAUTICAL RESEARCH LABS MELBOURNE (AUSTRALIA) F/G 1/3
LOAD SPECTRUM MEASURING EQUIPMENT. PART 2. DETAILS OF MK 2 SYST--ETC(U)
SEP 78 K F FRASER, U R KRIESER
UNCLASSIFIED ARL/MECH-ENG NOTE-372 NL

| OF |
AD A073350

END
DATE FILMED
9-79
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

ARL-MECH-ENG-NOTE-372

AR-001-303

DEPARTMENT OF DEFENCE

DEFENCE SCIENCE AND TECHNOLOGY ORGANISATION

AERONAUTICAL RESEARCH LABORATORIES

MELBOURNE, VICTORIA

MECHANICAL ENGINEERING NOTE 372

LOAD SPECTRUM MEASURING EQUIPMENT

PART 2 DETAILS OF MK 2 SYSTEM USED TO ACQUIRE TORQUE LOAD DATA IN SEA KING HELICOPTERS

by

K. F. FRASER and U. R. KRIESER

COPY No 22

SEPTEMBER 1978

AR-001-303

DEPARTMENT OF DEFENCE
DEFENCE SCIENCE AND TECHNOLOGY ORGANISATION
AERONAUTICAL RESEARCH LABORATORIES

(14) ARL/MECH-ENG NOTE-372

MECHANICAL ENGINEERING NOTE 372

(6)

LOAD SPECTRUM MEASURING EQUIPMENT.

PART 2. DETAILS OF MK 2 SYSTEM USED TO ACQUIRE TORQUE LOAD DATA IN SEA KING HELICOPTERS.

by

(10) K. F. FRASER and U. R. KRIESER

(12) 64 p.

(11) Sep 78

SUMMARY

Measuring equipment which uses a set of electromechanical counters to indicate either the integrated time in seconds for which torque loading on a transmission component falls within each of a number of bands or the number of times each of a number of torque-bands is traversed, is described. Separation of the torque level into bands is made possible using a single transducer, an amplifier with zero and gain adjustments for setting the extremes of the torque range of interest, an analogue to digital converter and decoder to separate the torque range into bands and counters to totalize the contributions relevant to each band.

POSTAL ADDRESS: Chief Superintendent, Aeronautical Research Laboratories,
Box 4331, P.O., Melbourne, Victoria, 3001, Australia.

CONTENTS

1. INTRODUCTION

Equipment which provides a readout of the totalized time that the torque, developed in the main rotor gearbox, falls within each of a number of bands, has been installed in some Wessex helicopters operated by the Royal Australian Navy (RAN). Complete details of that equipment are given elsewhere[1]. Two units installed in 1975 have been acquiring torque load data which have been used in the estimation of the safe fatigue life of critical gears in Wessex aircraft.

Since the program of gathering torque load data on Wessex helicopters was commenced the RAN has acquired a fleet of Sea King helicopters. Because reliable predictions on the safe fatigue life of transmission components greatly assist helicopter operators to plan overhaul schedules and formulate spares strategy, the RAN decided to install similar torque logging equipment in Sea King helicopters. Updated circuits, described in this report, have been used for this latter application. For identification purposes the equipment fitted in Wessex aircraft will be referred to as the Mk.1 Torque Analyser and that described here as the Mk.2 Torque Spectrum Indicator (or just "indicator").

Sea King helicopters are fitted with two engines which together contribute to the total torque transferred through the main rotor gearbox. In effect main rotor gearbox torque is approximately proportional to the sum of the individual torques developed by each engine. To make cockpit indication of developed torque possible a hydraulic torque sensing system is employed. The axial component of force transferred to a helical gear at the output of each engine is taken as a measure of torque output for the corresponding engine. This force is counter-balanced by a "cushion" of oil, its pressure being proportional to torque. The percentage of full load torque developed by each engine is indicated on cockpit meters (two needle). A pressure transmitter is used to transform the pressure signal into an equivalent synchro angle which is transmitted electrically to a receiving synchro in the cockpit torquemeter.

To sense torque for the application described herein pressure transducers have been mounted in the hydraulic torquemeter lines associated with each engine. With such an arrangement the system becomes independent of the aircraft pressure to synchro angle converter and can be calibrated prior to installation in the aircraft.

For the Sea King transmission system (up to and including the main rotor gearbox) there are three torques to be measured to allow computations to be made on the safe fatigue life of all relevant gears:

(i) Torque developed by port engine for gearing at the output of that engine.
(ii) Torque developed by starboard engine for gearing at the output of that engine.
(iii) Sum of individual engine torques for gearing in the main rotor gearbox.

To allow spectra corresponding to the above three torques to be measured three indicators are required. An initial installation comprising three indicators was commissioned in a Sea King helicopter in June 1978.

Functionally the system described is similar to that employed for the Mk.1 Analyser. However circuit details vary to provide:

(i) Modified input circuits to allow torque inputs to be summed.
(ii) Improved performance relative to the Mk.1 Analyser.
(iii) Increased versatility relative to the Mk.1 Analyser.
(iv) Reduced component count relative to that for comparable functions performed by the Mk.1 Analyser.
(v) Any updates considered desirable or necessary following experiences with the Mk.1 Analyser.

The updated indicator is a general purpose instrument with a wide range of applications. It need only be supplied with an analogue voltage signal proportional to torque, or whatever other quantity is to be totalized in the manner to be described. It can be used not only to indicate

total time for which torque falls within each of a number of bands but also (by alternative link selection) to indicate the number of times each of a number of levels or bands is traversed.

2. GENERAL DESCRIPTION OF LOAD SPECTRUM INDICATOR

A block schema of the system for torque load spectrum indication is given in Figure 1.

Sensors providing electrical outputs proportional to the torque developed by each engine are required. Strain gauge pressure transducers are inserted in each torquemeter pressure line (Sec. 1) for this purpose.

A separate instrument is required for the indication of torque loading on each engine. If the torque load spectrum for gears within the main rotor gearbox is required then the outputs of the two transducers must be suitably summed. To accommodate all these possibilities a 2-channel DC amplifier is used. When the two input signals are to be added a special link is inserted in the DC amplifier printed circuit board, otherwise with the link removed only one transducer output is analysed. A balance adjustment is necessary when the two transducer outputs are added. Zero and gain adjustments are provided in the output stage of the DC amplifier. These two adjustments set lower and upper limits for the torque range of interest and apart from the balance adjustment (where applicable) are the only adjustments necessary at the time of calibration.

To remove any high frequency noise components, or any torque components out of the frequency band of interest a filter is incorporated in the output stage of the DC amplifier.

Conversion of the analogue output of the DC amplifier to digital form is performed using an ADC (analogue to digital converter). In effect the 8-bit ADC allows the torque range of interest to be divided up into 256 steps (maximum) which may be suitably combined into torquebands.

A master crystal controlled clock signal is suitably divided in frequency to allow conversion command signals to be generated at the required rate for the ADC. Conversion rate is made sufficiently high to ensure that the input signal will never change much between successive conversion commands at the highest torque signal frequency of interest.

The torqueband separator (Fig. 1) allows operation in either of two modes (selectable via link connections on the printed circuit board):

(i) Torque duration totalizer (the time for which the torque falls within the specified band limits is totalized for each band).

(ii) Level exceedance totalizer (the number of times a torque level exceeds a certain specified value and subsequently drops below another specified value is totalized for a number of such pairs of levels).

For either system the appropriate band extremes are programmed into a plug-in ROM (read only memory). Each time a conversion is performed in the ADC the levels stored in the ROM are scanned and compared with the ADC output. In system (i) a pulse is transferred to the appropriate pre-counter after each conversion, but in system (ii) pulse transfer occurs only after a pair of band extremes have been traversed.

A pre-counter (Fig. 1) is effectively allocated for each band (i.e. a total of ten pre-counters). Counting takes place on a time-shared basis using a single counter the updated contents of which are successively loaded back into a 64-bit RAM (random access memory) which stores the ten pre-counter states in addresses 0 through 9. In addition the same counter and RAM are used as part of the programmer for:

(i) Dividing the frequency of the master clock signal, and thus setting the conversion rate of the ADC.

(ii) Setting the duration of the output pulses transferred to the electromechanical counters each time the capacity of a pre-counter is reached.

Output from the pre-counter printed circuit card is in the form of a 4-line address which corresponds to the address (0 through 9) of the readout to be advanced by one count. When no transfer is required dummy output address 15 is used.

A choice of link positions on the pre-counter printed circuit board allows the conversion rate of the ADC, the count range of the pre-counters, and the readout transfer pulse duration to be separately chosen over wide ranges. In general the link settings for the torque duration totalizer will be quite different from those used for the level exceedance totalizer.

Electromechanical readouts with decimal indication are used. These readouts increment by one each time their coils are energized. Other systems of storing totalized counts over long periods were considered (e.g. core memory, MOS memory etc.) but it was felt that the electromechanical readout was the best in this instance because:

(i) Totalized count readings are almost indestructible and no standby current is required for storage or display after a flight.

(ii) Totalized counts can be easily read at any time without the need for ancillary display equipment.

(iii) Because the system is required to handle only one channel of input data the overall storage requirement and the data rate requirement are well within the capacity of the electromechanical readout.

Regulated supplies of ± 15 V and $+5$ V are obtained from supply units using 115 VAC 400 Hz single-phase primary input power. Readouts and associated driver circuits are powered directly from the aircraft 28 VDC supply.

Transfer of the readout address to a 10-line decoder and readout driver is achieved via optical isolators. Internal circuit common and readout common are thereby isolated. One major advantage resulting from the use of the isolators is that DC supply currents are prevented from flowing back to the primary power source via the instrumentation chassis when internal circuit common is connected to that chassis.

A start synchronizing signal generator (Fig. 1) delays application of 28 VDC to the readouts and resets all pre-counters to the zero count state at the time 115 VAC is first applied. With this arrangement erroneous contributions in high torquebands at the time power is first applied are prevented.

3. DETAILED DESCRIPTION OF LOAD SPECTRUM INDICATOR

3.1 Transducer

As mentioned earlier (Sec. 1) pressure transducers are used to sense the torque developed by each engine in the Sea King helicopters. A strain gauge type providing response down to zero frequency has been adopted.

In the Sea King helicopters the cockpit torquemeters provide an indication range of 0 to 150% rated maximum torque which is equivalent to a torquemeter pressure range of 0 to 758 kPa (110 psi [pound per square inch]) approximately. To accommodate a range of 150% rated torque a transducer with a nominal full scale of 10 bar (145 psi) is adequate.

A Bell and Howell Model 4–800 with special vented gauge option is used. This transducer has the following salient characteristics.

(i) 10 VDC nominal excitation (15 VDC maximum).

(ii) 350 ohm nominal bridge resistance.

(iii) 30 mV nominal full scale output (for 10 bar pressure).

(iv) Natural frequency above 10 kHz.

(v) Non-linearity not greater than 0·3% of nominal full scale output.

(vi) Hysteresis less than 0·1% of nominal full scale output.

(vii) Compensated temperature range -54 to $+120$°C.

(viii) Operating temperature range -54 to $+150$°C.

(ix) Thermal zero shift within 0·009% full scale per °C over compensated range.

(x) Thermal sensitivity shift within 0·009% full scale per °C over compensated range.

(xi) Designed to operate in severe airborne environment (high vibration, shock or steady acceleration).

The choice of the above transducer represents a compromise between cost and performance. Based on the manufacturer's worst case drift figures a 0·5% shift in zero and a 0·5% shift in sensitivity could occur over a 55°C temperature range. It is essential that both the transducer and the indicator have low drift with temperature and time. Because these two items will be subject to different temperatures it is not possible to provide overall temperature compensation.

Excitation for the transducers is obtained from a balanced ± 5 V supply incorporated in the indicator (Sec. 3.2.2). To eliminate the effect of the transducer output lead length on the transducer output, sense leads are incorporated in the aircraft wiring. The voltage sense outputs (defined as V_{RP} SENSE and V_{RN} SENSE in Sec. 3.2.2) are joined to the normal current carrying outputs (V_{RP} and V_{RN}) at the connector which mates with the transducer.

3.2 Torque Spectrum Indicator

3.2.1 General

Each Torque Spectrum Indicator is constructed as a single instrumentation item which may be "hard" mounted in a helicopter. Ten non-resettable 8-digit readouts similar to those used in the Mk.1 Analyser are mounted on the front panel. This type of readout was extensively tested prior to and during commissioning of the Mk.1 analysers. The readouts have performed reliably since the analysers were commissioned.

The circuits require regulated ± 15 V and $+5$ V supplies. Suitable supply units incorporating transformer, rectifier and regulator sections are used to generate these using aircraft 115 VAC 400 Hz as primary power. As indicated earlier (Sec. 2) aircraft 28 VDC is used for the readouts and their driver circuits.

Circuits internal to the indicator are mounted on plug-in printed circuit boards. Four boards as summarized in the following table are used:

Board	Functional Description
A	Analogue Amplifier and Transducer Excitation Generator
B	Band Separator
C	Pre-Counter
D	Start Sync Generator and Output Driver Circuits

In the following sections circuit details will be given for each board. Complete information on the components used and the system of labelling adopted for the circuits is given in Appendix 1. Details of interconnections between printed circuit boards and other interwiring within the indicator are given in Appendix 2.

Each indicator is fitted with three connectors (J1 to J3 as indicated in Appendix 2) for the following functions:

(i) Power input.

(ii) Transducer input/output.

(iii) Output signal monitor.

When the torque loading in the main gearbox is to be measured the outputs of the two transducers, monitoring individual engine torque, are connected to the indicator via J2. The analogue sum of these outputs is generated within the indicator. When the two transducer connection applies, only one set of sense leads can be used.

To facilitate the calibration and checkout of the indicators the ADC output and some internal signals of interest are brought out on the output signal monitor connector (J3). With this arrangement the ADC output may be conveniently displayed using an ancillary display monitor (Sec. 4).

3.2.2 Analogue Amplifier and Transducer Excitation Generator

DC excitation of the strain gauge transducer is employed; hence a DC signal amplifier is required since the system must respond to steady state torque inputs. Both the amplifier and the reference supply for the transducer strain gauge bridge are included on printed circuit board *A* for which circuit details are given in Figure 2 and layout details in Figure 3.

A balanced (± 5 V) supply providing 10 V excitation is used. Such a balanced supply sets the common mode bridge output voltage to zero approximately. With this arrangement the amplifier output is virtually unaffected by any changes in amplifier common mode rejection with temperature.

Regulator Q1 (Fig. 2) and associated components provide the V_{RP} ($+5$ V) excitation. V_{RP} acts as reference for the V_{RN} (-5 V) excitation.

If in a particular application the only torque loading of interest were that developed in the main gearbox then one Torque Spectrum Indicator would be sufficient, but the outputs of

the two transducers sensing the torque output of each engine would need to be added. To accommodate this requirement the regulators have been designed to supply excitation to both transducers if necessary. Supply current for each transducer is about 30 mA. The regulators are protected in the event of either output being shorted.

Sense outputs V_{RP} SENSE and V_{RN} SENSE are provided. These are connected to V_{RP} and V_{RN} respectively at the transducer mating connector.

As the output of the strain gauge bridge is proportional to the excitation voltage it is essential that good stability be provided. In particular any changes with temperature should be minimized. Typical drift with temperature of the Q1 regulator is 0·003%/°C. Over a temperature range of 50°C a typical drift of about 0·15% can be inferred. Amplifier Q2 has sufficiently low offset drift with temperature to render that negligible in this instance. To achieve the rated performance of the regulator some high stability resistors must be used (refer to component list in Appendix 1). Some special selection of the Q1 regulator may be necessary as the worst case temperature drift is five times the typical value.

A dual-channel amplifier, to accommodate inputs from both transducers if necessary, is used. Identical input stages incorporating Q3 and Q4 respectively provide:

(i) Differential input.

(ii) High common mode rejection ratio (typically of the order of 100 dB over the frequency range 0 to 60 Hz) virtually unaffected by the values of gain determining resistors chosen over a wide range.

(iii) High input impedance.

(iv) High closed-loop gain capability (about 200 required for this stage) settable by two external resistors [for Q3 amplifier gain is (R19 + R20)/(R17 + R18)].

(v) Fairly low zero drift with temperature (1·5 μV/°C typical, 5 μV/°C maximum).

(vi) Adequate signal bandwidth (within 1% to about 10 kHz at a gain of 200).

Low input amplifier drift with temperature is a most important requirement. Because of drift problems[1] with the Mk.1 Analyser the input amplifier chosen for this application has improved performance in that respect. If full scale torque range of interest is represented by a change of 30 mV at the transducer output (a nominal 75 psi change at the transducer input) then the input amplifier drift referred to that full scale input becomes 0·005%/°C typical or 0·017%/°C maximum (referring to item (v) above). Recent measurements on four devices (type AD521K) at these laboratories revealed zero drift over the temperature range −25 to +55°C of 0·14%, 0·44%, 0·44% and 0·46% relative to a 30 mV full scale input.

Q5 and associated components form a summing amplifier with nominal unity gain for the average of the two inputs. When only one transducer output is to be processed, connection is made via the *A* inputs (to Q3) and the link at the output of amplifier Q4 is left open. When the sum torque is of interest, the second transducer output is connected via the *B* inputs (to Q4) and the link is shorted. By changing the gain of this stage from 1 to 0·5 when a change is made from a single input to a dual input system the output of the summing amplifier is normalized. Potentiometer R44 allows overall sensitivity for each torque measuring channel to be equalized.

The final amplifier stage incorporating Q6 and associated components has provision for large zero shift. Potentiometers R33 (coarse) and R34 (fine) allow the amplifier zero to be trimmed whereas R26 (fine) and R27 (coarse) allow the overall gain to be trimmed. DC gain of the stage is nominally set to about 2. As the output of this amplifier is coupled to the ADC input (Sec. 3.2.3) having a full scale input of 10 V, the zero and gain are trimmed at the time of calibration to provide outputs close to 0 V and 10 V at the lower and upper extremes respectively of the torque range of interest. Actual levels for setting purposes are a function of the ADC digital outputs chosen to represent the extremes of the band of interest.

As the amplifier zero shift is derived from the transducer excitation supplies (V_{RP} SENSE and V_{RN} SENSE) any variation in these supplies will result in a zero shift at the amplifier output. Based on a gain factor of about 1·5 (an approximate figure for components indicated in Fig. 2) for the zero shifting circuit a change of +0·15% in the transducer excitation (a typical figure predicted for a 50°C temperature change) would result in a change of −0·11% of full scale output (assumed to be about 10 V). Any zero offsets in amplifiers Q3, Q4 or Q5 are taken care of in the overall zero adjustment.

To achieve the requisite high stability of the completed amplifier, with respect to both zero and gain, many high stability resistors are required (refer to component list in Appendix 1).

A filter comprising a single low pass section (involving R26 to R30, C17 to C20) in the forward path and a resistor shunt bridged-T network in the feedback path of the final amplifier has been selected. Characteristics of such a filter have been examined in detail for the Mk.1 Analyser[1]. Any high frequency noise components and any signal components outside the frequency band of interest may be removed with this filter.

Some in-flight measurements have been made on a number of Sea King helicopters to determine the extent of dynamic components present in the torque transmitter pressure signal and assess the low pass filter requirements. It has been decided the fundamental component at the blade passing frequency (17 Hz nominal)be passed without attenuation. The most significant dynamic component noted in the tests had a frequency of about 54 Hz (main drive shaft frequency) and had an amplitude equivalent to 10% rated torque peak to peak at 110% steady torque setting. It was felt that this component did not reflect a true component of torque and therefore should be attenuated (dynamic components of significant amplitude can cause incorrect advance of readings on high band counters). Characterists of the Mk.2 filter have been made virtually the same as those for the Mk.1 circuit. Salient features are summarized below:

(i) Response flat within 8% from 0 to 21 Hz.
(ii) Response 3 dB down (i.e. 70% of "zero" frequency value) at 24 Hz.
(iii) Response 20 dB down (a factor of 10) at 53 Hz.
(iv) Response 40 dB down (a factor of 100) at 135 Hz.

Where resistance or capacitance values are critical a series or parallel connection of components has been specified as indicated in the circuit of Figure 2.

Components indicated in the circuit of Figure 2 have been chosen to provide 0·00 V output at 2·6% rated torque (1·9 psi pressure) and +10·00 V full scale at 156·2% rated torque (equivalent to 114.5 psi pressure). Extremes of each torqueband may be set anywhere in the range 3·2% to 146·6% rated torque with 0·6% resolution using the ROM plug-in for the band separator (Sec. 3.2.3). If the low limit on the lowest band is made 3·2% of rated torque or above no readout changes will occur unless 3·2% or greater torque is developed.

3.2.3 Band Separator

Complete circuit and layout details for the band separator are given in Figures 4 and 5 respectively, and waveforms at various points marked on this circuit are given in Figure 6.

Two distinct operating modes are possible:

(i) When link LK1 is placed in position 1 the band separator will provide an output corresponding to the address of the band (0 to 9) within which the ADC output falls each time a conversion takes place. A conversion rate of 1·024 kHz has been adopted for the Mk.2 indicator so that, in that case, if the number of times each address appears at the output is counted a totalized count of 1024 for any band will indicate that the torque has resided in that band for a period of 1 second. For simplicity, operation in this mode will be referred to as "torque duration indication".
(ii) When link LK1 is placed in position 2 the band separator will provide an output corresponding to the address of the band (0 to 9) each time a full traverse of the band occurs. Hence the appearance of an address (in the 0 to 9 range) at the output indicates that another "fatigue cycle" in the relevant band is to be counted. For simplicity, operation in this mode will be referred to as "level exceedance indication".

To enable the torque duration for each band to be accurately estimated conversions in the ADC must occur at a stable and accurately known repetition rate. To meet this requirement a crystal oscillator comprising XL1 and associated components (Fig. 4) is used to provide a master clock for all timing functions. A crystal frequency of 2·097152 MHz has been chosen (where $2{\cdot}097152 \times 10^6 = 2^{21}$). The frequency of the master clock is divided by 2 via counter Q10 and the resulting HF CLK (waveform 1 of Fig. 6) is taken to the pre-counter (Sec. 3.2.4) where the frequency is further divided and used to time various program functions. Although accurate timing is not required for the level exceedance indicator the same master clock is used for that system also.

Two timing signals, GATE and LF CLK (waveforms 2 and 3 of Fig. 6), derived from the master clock after frequency division in the pre-counter are received as inputs to the band separator. To simplify discussions on timing the repetition period of the HF CLK will be defined

as T (i.e. T = 0·9537 μs). The GATE signal has a repetition frequency of 2·048 kHz; the signal level is high for 8T and low for 504 T. At each negative transition of the GATE signal a negative going STROBE 1 pulse (waveform 3 of Fig. 6) of 230 ns nominal duration is generated. The LF CLK signal is a 1·024 kHz square wave. Each time the LF CLK switches low a positive going conversion trigger (waveform 7 of Fig. 6) of 230 ns nominal duration is transferred to the ADC.

The analogue amplifier output (Sec. 3.2.2) is connected to the ADC analogue input. Unipolar operation (0 to + 10 V full scale) is used in the Mk.2 indicator but potentiometer R1 and link have been provided to allow bipolar operation (−5 V to + 5 V full scale) if that is ever desired. When the START CONVERT input switches high the ADC outputs are reset to the 0 state. A conversion starts on the negative transition of that input and is complete within about 4 μs. An 8-bit straight binary coded output is generated.

Operation of the band separator for torque duration indication will be considered first. In the first 20 addresses (designated 0 through 19) of the ROM, numbers used to specify upper and lower limits of each torqueband are stored. Actually a number equal to the ADC output which corresponds to the upper limit for each band is stored at the even addresses, and a number equal to the lower limit of each band is stored at the odd addresses. Even addresses 0 through 18 are allocated for storage of the upper limits of bands 1 through 10 respectively and odd addresses 1 through 19 for storage of the lower limits of bands 1 through 10. If the band number is designated by the symbol R (i.e. $1 \leqslant R \leqslant 10$) and if the band limits are defined as N_{1R} and N_{2R} where, for torque duration indication, N_{1R} is the upper band limit and N_{2R} the lower band limit then the ROM program defined in the following table will be required.

Band	Requisite Band Limits (as Meas. at ADC Output)	Requisite ROM Program	
		Address	Number Stored
R	N_{1R}	2(R − 1)	N_{1R}
	N_{2R}	2 R − 1	N_{2R}

Designating the ADC output as N it follows that if $N \leqslant N_{1R}$ and $N \geqslant N_{2R}$ then $N_{1R} \geqslant N \geqslant N_{2R}$ and N is within band R. By successively checking for each band until the above condition is satisfied the correct band can be established.

The programming requirement can be most readily illustrated with an example. The torqueband settings initially adopted for the summation torque spectrum for Sea King helicopters are used in the following table.

Band	Torqueband Range (per cent Rated Torque)	ADC Output* Range (Decimal)	Requisite ROM Program	
			Address (Decimal)	No Stored (Decimal)
1	5–47	4–73	0 1	73 4
2	47–71	74–113	2 3	113 74
3	71–83	114–133	4 5	133 114
4	83–95	134–153	6 7	153 134
5	95–101	154–163	8 9	163 154
6	101–107	164–173	10 11	173 164
7	107–113	174–183	12 13	183 174
8	113–119	184–193	14 15	193 184
9	119–125	194–203	16 17	203 194
10	> 125	204–255	18 19	255 204

* In this case the analogue amplifier is adjusted to provide an ADC output of $3 \rightarrow 4$ (just switching) for 4% applied torque (or equivalent calibration signal) and $251 \rightarrow 252$ for 125% applied torque (or equivalent calibration signal).

For the particular program indicated in the previous table only torques greater than or equal to 4% rated torque will fall within the 10 specified bands. If the torque falls below the 4% figure no output will be transferred to any of the electromechanical counters (as will become clear in due course). Such a program has the advantage that no output is generated on the lowest band during ground checks with engines not running. Similarly if the torque drops below the 4% figure during flight (e.g. during autorotation) no output will be generated and some difference between the change in the totalized times registered by the band counters and total operating time may result. If agreement between the total operating time and the change in the totalized times registered by the 10 readouts were considered desirable (for checking purposes) then the first band could have been set to "<47% rated torque" for which the ADC output range would be $0 \rightarrow 73$. For a torque lower than that which just produces an ADC output of 0 the ADC output will remain fixed at 0, and similarly for a torque greater than that which just produces an ADC output of 255 the ADC output will remain fixed at 255.

It is to be noted that only 20 of the available 32 addresses in ROM Q9 are used for storage of the torqueband limits. For the type DM8578N ROM (Fig. 4) all unprogrammed bits have

a high value. Hence 255 will be effectively stored at addresses 20 to 31. If the band 10 limit were set to 254 or lower then an ADC output of 255 (resulting from a high level torque) would not fall within any of the 10 specified bands. However the ADC output would fall within the "phantom" band specified by each pair of unprogrammed addresses. An output would be generated at band separator address 10 (addresses 0 to 9 correspond to bands 1 to 10) but since address 10 is never examined in the pre-counter (Sec. 3.2.4) no malfunction will result, so unused addresses may be left unprogrammed. Similarly for an alternative ROM (e.g. type 82S123 as indicated in Appendix 1.2) having all unprogrammed bits low, no malfunction will result if unused bits are left unprogrammed.

NOR gates Q16A and Q16B enable the additional "equal to" condition to be included when the ADC and ROM outputs are compared. The only reason for utilizing the "equal to" condition is to allow over-range bands (e.g. $>125\%$ torque) and under-range bands (e.g. $<4\%$ torque) to be selected for bands 10 and 1 respectively.

For each cycle of the LF CLK the following sequence of operations applies for the torque duration indicator:

(i) Counters Q10 and Q13, and flip flop Q15A (the first in the dual flip flop device Q15) are initially cleared via the RESET pulse (waveform 6 of Fig. 6) which is generated at the time of the negative transition of the gate input but only when the LF CLK is high. STROBE 2 (waveform 8 of Fig. 6) together with outputs B and C (waveforms 9 and 10 of Fig. 6) of Q10 is taken to demultiplexer Q11 which generates control outputs indicated in waveforms 11 to 16 of Fig. 6. Output C of Q10 forms the least significant bit of the 5-bit ROM address; outputs of Q13 form the remaining four ROM address bits.

(ii) With the counters cleared as in (i) ROM address 0 is chosen.

(iii) During the first half of the period during which address 0 is chosen flip flop Q15B (the second flip flop in the Q15 device) is preset under the action of the 1Y0 output (waveform 11 of Fig. 6) through NOR gate Q12C and AND gate Q5B. Each time an even ROM address is chosen Q15B is preset in the same manner. If at the time of arrival of the preset pulse the Q2 output of flip flop Q15 is high no change of state will occur.

(iv) The contents of ROM address 0 are compared with the output from the ADC via the magnitude comparators Q7 and Q8. If the ADC output is less than or equal to the ROM output a clear pulse (waveform 19 of Fig. 6) will be transferred to flip flop Q15B during the latter half of the period for which ROM address 0 is chosen; otherwise no clear pulse will be generated.

(v) ROM address 1 is chosen.

(vi) The contents of ROM address 1 are compared with the output from the ADC. If the ADC output is greater than or equal to the ROM output a preset pulse (waveform 18 of Fig. 6) will be transferred to flip flop Q15B during the first half of the period for which address 1 is chosen, otherwise no preset pulse will be generated. If, when the preset pulse is generated, flip flop Q15B changes state it follows that the ADC output lies between the values stored in ROM addresses 0 and 1 and hence indicates that an increment is to be added to the channel 1 pre-counter. A change of state of the Q15B output (waveform 20 of Fig. 6) at this time will cause the output (waveform 21 of Fig. 6) of NAND gate Q3C to switch low for a period of 230 ns nominally and clear flip flop Q15A (set Q1 output high). As a consequence further counting in Q13 will be inhibited (CE input high) thus "freezing" the output address at 0 in this instance.

(vii) If the Q15B flip flop does not change state as indicated in (vi) ROM address advancing will continue with the same sequence of operations for even addresses as for address 0 and for odd addresses as for address 1. The addresses will advance until the correct band is located at which time the output address will be "frozen" as in (vi).

(viii) For torque duration indication the action of RAM Q14 is not relevant.

(ix) After half of an LF CLK repetition period has elapsed since the previous RESET pulse (waveform 6 of Fig. 6) was generated a START CONVERT pulse (waveform 7 of Fig. 6) is generated thus initiating a new conversion. At this stage the ADC output

is not examined; such examination takes place when initiated by the next RESET pulse as detailed in (i).

(x) For the period when both the GATE and LF CLK are high, which occurs just before the next RESET pulse initiates the next cycle, the tri-state address output of Q13 is enabled thus transferring the appropriate band address (0 through 9 corresponding to bands 1 to 10) to the pre-counter. It follows that the transfer of the band address takes place about 1·5 repetition periods of the LF CLK after the corresponding conversion was initiated (refer to waveforms 2 to 7 of Fig. 6).

For the torque duration indication the maximum time taken to locate the correct band is 20 T (about 20 μs being the duration of 20 cycles of the HF CLK).

Operation of the band separator for level exceedance indication is somewhat different and will now be examined in detail.

Each band is once again allocated two levels. If the torque exceeds the higher level and some time later falls below the lower level an extra count (or "fatigue cycle") is to be added to the number stored for that band. Once again the numbers stored in the ROM define the upper and lower limits for each band. However in this instance the lower numbers will be stored at the even ROM addresses and the higher numbers at the odd addresses. Overlapping of bands is quite feasible, but the upper and lower limits must not be set to the same value.

Once again let us designate the band number by the symbol R and the band limits by N_{1R} and N_{2R} where, in this instance, N_{1R} is the lower band limit and N_{2R} the upper limit. If N is the ADC output then for each conversion and for each band the validity of $N \leqslant N_{1R}$ and $N \geqslant N_{2R}$ is checked. For any given ADC output both these conditions can never be simultaneously satisfied. Consider that storage is provided for an information bit L which takes on a logical 0 value if condition $N \leqslant N_{1R}$ is satisfied and maintains that value until condition $N \geqslant N_{2R}$ is satisfied at which time L will switch to a logical 1 and maintain that value until condition $N \leqslant N_{1R}$ is next satisfied. A change in state of the L bit will therefore only occur once per complete traverse of the relevant band and may be used to indicate that another fatigue cycle is to be counted. The above procedure is employed in the band separator when it is used for level exceedance indication.

By varying the ROM program the level exceedance indicator may take various forms. In the following table the exceedance of 10 distinct levels is considered. Provided the torque drops by 5% (of rated torque) before the level is exceeded again another cycle will be counted.

Band	Upper Limit (per cent rated torque)	Lower Limit (per cent rated torque)
1	40	35
2	50	45
3	60	55
4	70	65
5	80	75
6	90	85
7	100	95
8	110	105
9	120	115
10	130	125

A system which has found favour in the estimation of fatigue damage on components or structures is one employing the Range Pair count method[2]. With this system the presence of either large or small load fluctuations is never ignored and large variation cycles are not counted too often. A number of reference levels are specified and variation cycles between all possible pairs of reference levels are counted. For an n reference level range it can be easily shown that there are $n(n-1)/2$ possible Range Pairs. Each Range Pair requires separate storage. Thus for a 5 level range exactly 10 pairs are possible and a 10 readout system, as provided in this instance, is required. Consider that the reference levels tabulated below are chosen.

Reference Levels (per cent rated torque)	30	68	96	116	130

To indicate cycles for each Range Pair a ROM program as illustrated in the following table could be used.

Band	Torque Range Pair (per cent rated torque)	ADC* Output (Decimal)	Requisite ROM Program	
			Address (Decimal)	No. Stored (Decimal)
1	30 68	2 97	0 1	2 97
2	68 96	97 167	2 3	97 167
3	96 116	167 217	4 5	167 217
4	116 130	217 252	6 7	217 252
5	30 96	2 167	8 9	2 167
6	68 116	97 217	10 11	97 217
7	96 130	167 252	12 13	167 252
8	30 116	2 217	14 15	2 217
9	68 130	97 252	16 17	97 252
10	30 130	2 252	18 19	2 252

* In this case the analogue amplifier is adjusted to provide an output $1 \rightarrow 2$ (just switching) from the ADC for 30% applied torque (or equivalent calibration signal) and $251 \rightarrow 252$ for 130% applied torque (or equivalent calibration signal).

For level exceedance indication the following sequence of operations takes place in the band separator:

(i) Counters Q10 and Q13, and flip flop Q15A are initially cleared via the RESET pulse as for the torque duration indicator.

(ii) ROM address 0 is chosen.

(iii) The state (1 or 0) stored at address 0 of the RAM Q14 is read and transferred to the Q2 output of flip flop Q15B during the first half of the period during which

ROM address 0 is selected. Transfer is controlled by the CLK2 signal (waveform 17 of Fig. 6).

(iv) The contents of ROM address 0 are compared with the output from the ADC. If the ADC output is less than or equal to the ROM output a clear pulse (waveform 19 of Fig. 6) will be transferred to flip flop Q15B during the latter half of the period for which ROM address 0 is chosen; otherwise no clear pulse will be generated.

(v) ROM address 1 is chosen.

(vi) The contents of ROM address 1 are compared with the output from the ADC. If the ADC output is greater than or equal to the ROM output a preset pulse (waveform 18 of Fig. 6) will be transferred to flip flop Q15B during the first half of the period for which address 1 is chosen, otherwise no preset pulse will be generated. It is not possible for a clear pulse as in (iv) and a preset pulse as above to be both generated for any given ADC output as that output cannot be simultaneously less than or equal to 2 and greater than or equal to 97 (refer to above table). If, when a preset pulse is generated, flip flop Q15B changes state a clear pulse will be transferred to flip flop Q15A which in turn will inhibit any further counting in Q13, thus "freezing" the output address at 0 in this case.

(vii) During the latter half of the period for which ROM address 1 is chosen the state of flip flop Q15B is written (waveform 14 of Fig. 6) into address 0 of RAM where it will remain until the next band separation cycle (about 1 ms later for LF CLK frequency of 1·024 kHz). Hence a clear pulse will be transferred to Q15A as in (vi) only if one complete fatigue cycle has occurred (i.e. ADC output less than or equal to contents of ROM address 0 was detected on the previous band separation cycle and ADC output greater than or equal to contents of ROM address 1 has now been detected).

(viii) If flip flop Q15B does not change state as in (vi) the ROM will be consecutively addressed with the same sequence of operations for even addresses as for address 0 and for odd addresses as for address 1. The addressing will advance until either the completion of another fatigue cycle is registered as in (vi) or the counter outputs advance to output address 15. With the level exceedance indicator the non-detection of a completed fatigue cycle will occur for most band separation cycles. When output address 15 is generated the MAX COUNT output (waveform 22 of Fig. 6) of Q13 will switch low causing the CE (count enable) input to also switch low (waveform 23 of Fig. 6) thus inhibiting any further changes in output address until the next band separation cycle.

(ix) After half an LF CLK repetition period has elapsed since the previous RESET pulse was generated a new conversion is initiated in the ADC. Remarks as in (ix) for the torque duration indicator apply.

(x) For the period when both the GATE and LF CLK are high, which occurs just before the next RESET pulse initiates the next band separation cycle, the tri-state address output of Q13 is enabled thus transferring the output address (0 through 9 corresponding to bands 1 to 10, or 15 corresponding to a dummy address which leads to no increase in the fatigue cycle count).

For the Range Pair example cited above a full scale torque fluctuation (30 to 130%) will give rise to a contribution in each band. For a fluctuation cycle of lower amplitude an output will occur on all Range Pairs within the bounds of the fluctuation cycle. For any given band separation cycle (occurs at 1·024 kHz repetition rate) only one address output is possible; outputs for other bands would occur on later cycles. The band separator is capable of providing an output from each of the 10 bands in about 10 ms. However the electromechanical readouts limit (Sec. 3.2.4) the maximum fluctuation rate that can be handled. If, for example, the number of times that a traverse of not more than that defined by the band 1 Range Pair is required, then the sum of the entries on readouts 5, 8 and 10 (refer to previous table) would need to be subtracted from that of readout 1.

As indicated earlier all unprogrammed bits for ROM Q9 are high so that unused addresses (20 to 31 in this instance) would have the number 255 stored if unprogrammed. If full scale or an over-range input is applied to the ADC, the output will switch to state 255. Hence if a new fatigue cycle is not detected as ROM addresses 0 to 19 are scanned a "phantom" one will be

detected when ROM addresses 20 and 21 (corresponding to band separator address 10) are examined as the conditions $N \leqslant 255$ and $N > 255$ will be both satisfied in the same band separator cycle. Hence address 10 will be coupled to the band separator output. As address 10 in the pre-counter (Sec. 3.2.4) is a dummy one the contents of which are never examined, no malfunction occurs. Similarly for ROMs having all unprogrammed bits low, address 10 will be coupled to the band separator output when a zero or under-range input is applied to the ADC (resulting in ADC output of 0). Hence correct operation will result if unused ROM addresses 20 to 31 are left unprogrammed.

The START SYNC input (Sec. 3.2.5) switches high for a small delay starting at the time power is first applied. It then switches low, a state which is maintained until the next power interrupt occurs. A preset pulse for flip flop Q15B is generated for each odd ROM address selected while the START SYNC is high. Thus bit L stored in the RAM at addresses 0 through 9 is initially set high so that, for level exceedance operation, complete fatigue cycles will be required, after the START SYNC reverts to the low state, before an output is generated.

The 8-line ADC output is brought out so that numerical display of that output using ancillary display equipment is possible. Such display facilitates the trimming of the potentiometers in the analogue amplifier.

3.2.4 Pre-Counter

Complete circuit and layout details for the pre-counter are given in Figures 7 and 8 respectively, and waveforms at various points marked on that circuit are given in Figures 9 and 10. This circuit will handle band separator outputs when that separator is connected for either torque duration indication or level exceedance indication. However the requirements of the pre-counter circuit differ somewhat for these alternative modes of operation; optional link positions on the pre-counter allow the different requirements to be accommodated. When the torque duration indication mode is employed, a pre-counter division factor of 1024 is a typical requirement (assuming 1·024 kHz conversion rate). Such a division factor results in an output pulse being generated for each second of totalized time measured for any given channel. On the other hand, when the level exceedance indication mode is employed, the readouts normally need to be updated for each complete fatigue cycle indicated via the band separator output, and thus a pre-counter division factor of unity represents a normal requirement in this case. Considerable versatility is provided by optional links which allow the following to be preset:

(i) Analogue to digital conversion rate.
(ii) Pre-counter division factor.
(iii) Duration of readout pulse.

As indicated earlier (Sec. 2) the pre-counter utilizes a single counter operated on a time shared basis with the individual readings stored in a random access memory which is regularly updated. Devices Q5, Q9 and Q12 constitute the RAM which provides 12-bit storage for up to 16 inputs (but not all input channels are utilized). For convenience the addresses will be referred to as 0 through 15. Address allocation for the RAM is as follows:

(i) Addresses 0 to 9 for pre-counter storage as required for bands 1 to 10 respectively.
(ii) Address 12 for storage of successive readings of the HF CLK frequency divider.
(iii) Address 13 for storage of successive readings of a frequency divider used to set duration of output pulse delivered to readouts.

Addresses 10, 11 and 14 are not utilized, and 15 is used to accept dummy inputs (Sec. 3.2.3) but its contents are never interrogated. In special circumstances (Sec. 3.2.3) address 10 may receive dummy inputs.

The time-shared counter comprising devices Q6, Q10 and Q13 has 12-bit capacity (straight binary). The RAM output may be loaded in parallel into this counter.

In order to utilize the RAM and the counter to provide multiple channel counting a considerable number of additional devices is required for programming purposes. Programming details will now be considered.

Counter Q22 divides the frequency of the incoming HF CLK (waveform 1 of Fig. 9) by 8 and produces a 3-line output (waveforms 2, 3 and 4 of Fig. 9). Strobe pulses (waveform 5 of Fig. 6) of 230 ns nominal duration are generated at the high frequency clock rate (1·048576 MHz) but half an HF CLK period out of phase with the switching of the divide-by-8 counter. Under the

gating action of the strobe the 3-line counter output is decoded via Q23 to produce an 8-line output D1 to D7 (waveforms 6 to 13 of Fig. 9). Pulses (of 230 ns duration) are generated at 131·072 kHz repetition frequency (repetition period 8T) on each output line.

A complete memory cycle (read, update, count and write) takes 8T; thus the memory is accessed at a 131·072 kHz rate. Decoder outputs D0 to D7 form clock pulses for initiating the various program functions which take place during a memory cycle. These functions in order of occurrence in a memory cycle are listed in the following table.

Control Output From Decoder	Program Function Which Is Controlled
D1	* Select new RAM address
D2	Load contents of memory into time-shared counter (LOAD 1)
D3	* Advance time-shared counter by one count
D4	* Examine state of time-shared counter
D5	* Reset time-shared counter
D6	Write contents of time-shared counter back into memory (WRITE 1)
D7	Load contents of memory into time-shared counter (LOAD 2)
D0	Write contents of time-shared counter back into memory (WRITE 2)

* One or more of these actions is omitted in some memory cycles.

An appropriate WRITE ENABLE input (waveform 14 of Fig. 6) is generated by combining the D6 and D0 outputs from the decoder, and an appropriate MEMORY ENABLE input (waveform 15 of Fig. 9) is generated by combining the WRITE ENABLE input with suitable outputs from the 3-bit counter. Data are read from the memory, as indicated by the dotted signal in Figure 6 when WE + ME = 0 (where WE and ME are the WRITE and MEMORY ENABLE inputs respectively).

Because the inverse of what is written in the RAM appears on the output when the contents of the memory are read it has been found convenient to add the second LOAD and WRITE functions solely to achieve a net non-inversion over a complete memory cycle.

Most memory cycles are utilized for frequency division of the HF CLK. The generation of a GATE output (Sec. 3.2.3) having a repetition frequency equal to twice the required conversion frequency is a requirement. To enable a 1·024 kHz conversion rate to be achieved an overall division of the HF CLK frequency by a factor of 1024 is required. To produce the GATE signal a division factor of 512 is required. As there is one memory cycle for every eight cycles of the HF CLK a cycle of the GATE output is required for every 64 memory cycles. In effect 63 of the 64 memory cycles in question are used for the above frequency division and the remaining one for all other functions.

To examine the method by which the frequency of the HF CLK is divided assume that the GATE E3 (Fig. 7) is initially low. In that case the 1Q output of flip flop Q21A (where Q21A is the first and Q21B the second flip flop in the dual flip flop device Q21) must be low. Under these conditions tri-state buffer Q1 will be enabled and the hard-wired address 12 input to that device will be transferred to the RAM address bus. At other times the RAM address bus will receive inputs from other sources with tri-state outputs. At this time it may be assumed that the outputs from all other such sources are in the high impedance state. Further details on the address bus will be given shortly.

It follows that while GATE E3 is low RAM address 12 (indicated earlier as the address allocated for HF CLK frequency division) will be chosen. During each memory cycle the stored data in RAM address 12 will be loaded into the time-shared counter which will have its count state advanced by unity. Such counting will proceed until the counter output (waveform 16 of Fig. 9), coupled via link to the P6 terminal, switches high when the count state is advanced by unity. In Fig. 7 P6 is shown linked to P18 which is the 2^7 output of the time shared counter. If the counter were initially reset to the zero count state that output would switch high after 2^6

(i.e. 64) pulses had been received. Details on the time variation of the counter state and the number stored at address 12 of the RAM are shown under waveform 19 of Fig. 9. The following sequence of operations takes place during the memory cycle for which the count is advanced from state 63 to 64:

(i) At D2 (waveform 7 of Fig. 9) count state 63 will be read into the time-shared counter from RAM address 12.

(ii) At D3 the count state will be advanced to 64 resulting in the output E1 at terminal P6 switching high.

(iii) At D4 the state of E1 will be interrogated and because it is now high the E2 output (waveform 17 of Fig. 9) of the flip flop comprising NAND gates Q18A and Q18B will switch high.

(iv) Because E2 is now high the output of AND gate Q20B will be low thus causing a reset pulse to be transferred to the time-shared counter via NOR gate Q14D at D5.

(v) At D6 the contents of the time-shared counter (with the exception of the least significant bit) will be written into the RAM. Because E2 is high and the C output (waveform 3 of Fig. 9) of counter Q22 is also high at the time of arrival of D6, output E4 (waveform 19 of Fig. 9) will be high and hence also the output of NOR gate Q4C. Thus a "1" rather than a "0" will be transferred into the least significant bit of the RAM memory. Hence the count state effectively advances twice during this memory cycle.

(vi) At D7 the contents of the memory are read in inverted form back into the time-shared counter.

(vii) At D0 the counter outputs are written back into memory but at this time no inversion takes place via NOR gate Q4C.

(viii) At D1 (next memory cycle) the 1Q output of flip flop Q21 and hence also the GATE output E3 (waveform 18 of Fig. 9) will switch high resulting in the selection of RAM addresses other than 12. The selection of such addresses will be examined subsequently.

(ix) At D2 E2 will be reset to the low state. The sequence of operations for the memory cycle applicable to the new address will start.

(x) At the following D1, flip flop Q21A will be reset thus causing GATE E3 to switch back to the low state. RAM address 12 will now be chosen again.

(xi) At D2 the contents (state 1 as indicated in (v)) of the RAM will be loaded into the time-shared counter. After 63 memory cycles the sequence starting at (i) will be repeated. Thus the repetition period of the GATE E3 will be the duration of 64 memory cycles (512T) and the time for which it is high will be the duration of 1 memory cycle (8T).

Output E3 (waveform 21 of Fig. 10) of flip flop Q21A is taken to the divide-by-two section of counter Q22. The resulting square wave output is buffered via Q4B to produce the LF CLK signal (waveform 20 of Fig. 10). Both the GATE E3 and the LF CLK E5 are taken to the band separator. Conversion in the ADC takes place at the LF CLK repetition frequency (Sec. 3.2.3). When terminal P6 is linked to terminal P18 as shown in Figure 7 the resulting LF CLK frequency is 1·024 kHz. Other frequencies can be chosen simply by changing the link position. In the following table the LF CLK rate f_L (equal to half the repetition frequency of GATE E3) is given as a function of the link position.

LF CLK Details		Terminal to be Linked to P6
Repetition Frequency (f_L)	Repetition Period (T_L)	
*32·768 kHz (2^{15})	32T	P28
*16·384 kHz (2^{14})	64T	P26
8·192 kHz (2^{13})	128T	P24
4·096 kHz (2^{12})	256T	P22
2·048 kHz (2^{11})	512T	P20
1·024 kHz (2^{10})	1024T	P18
512 Hz (2^{9})	2048T	P16
256 Hz (2^{8})	4096T	P14
128 Hz (2^{7})	8192T	P12
64 Hz (2^{6})	16384T	P10
32 Hz (2^{5})	32768T	P8

* These frequencies are too high for the band separator of Figure 3, hence connection of P6 to P26 or P28 is not valid.

Consideration will now be given to the sequence of addresses which is applied to the RAM address bus driven in a time-shared manner by a number of devices with tri-state outputs. As indicated above, address 12 will be selected when GATE E3 is low (or when E3 is high as indicated in waveform 21 of Fig. 10). As indicated in Section 3.2.3 the 4-line band separator address output, which is connected to the RAM address bus, will be enabled if GATE E3 and LF CLK E5 are both 1 (Refer to waveforms 2, 4 and 5 of Fig. 6, and to waveforms 18, 20 and the band separator address select waveform of Fig. 10). When the band separator address is selected the number stored in the equivalent RAM address will be increased by 1 during the memory cycle for which both E3 and E5 are high. When GATE E3 is high and the LF CLK E5 is low either a clocked output address (0 to 9) or address 13 (for output pulse generation) will be selected as indicated by the "Clocked or RAM Address 13 Select" waveform of Figure 10.

The sequence of operations which leads to the generation of an output pulse for a readout is as follows.

When the band separator address is selected the number stored in one of addresses 0 to 9 or 15 is increased by unity at the LF CLK rate (1·024 kHz for the P6 to P18 link dotted in Fig. 7). In effect these numbers represent the individual pre-counter readings for the respective bands (except that, as indicated earlier, address 15 is a dummy). Examination of the pre-counter states is not accomplished at the time the band separator generates an output on the RAM address input.

While the tri-state 4-line BCD output address (OAD-1 to OAD-8) from decade counter Q3 is enabled an output pulse (Sec. 3.2.5) will be transferred to the readout having that address (0 to 9 corresponding to bands 1 to 10). For an additional interval, which sets minimum pulse separation, no examination of the pre-counter states occurs and no further output pulse can be generated. At times other than when an output pulse or the subsequent separation gap is being generated the numbers stored in RAM addresses 0 to 9 will be examined in turn at the LF CLK rate f_L while GATE E3 is high and the LF CLK low. Thus the time taken to interrogate all ten

addresses will be $10/f_L$. Interrogation in this manner will continue until a RAM address is found for which the stored contents exceed a prescribed number, N_P say. For the link positions indicated in Figure 7 the prescribed number is 1024, which for torque duration indication represents 1 second of integrated time. When a RAM address, for which the stored number is equal to or greater than N_P, is found that address will be "frozen" in decade counter Q3 for an appropriate interval while the relevant readout is energized. The subsequent minimum pulse separation interval has been made equal to the readout pulse duration.

The actual sequence of logical steps which give rise to the above operation will now be examined in detail.

As a starting point assume CONTROL GATE E6 (waveform 22 of Fig. 10) is low. It follows that the SELECT input to digital multiplexer Q2 will be high and the 4-line clocked address output from decade counter Q3 will be selected via the multiplexer. When GATE E3 is high and the LF CLK E5 is low the tri-state outputs of multiplexer Q2 will be enabled thus transferring the address output of decade counter Q3 to the RAM address bus.

A memory cycle at the chosen address will be initiated. At D2 the contents of that address will be read into the time-shared counter. At D3 a count advance will be inhibited via Q14C. Logically the advance is inhibited if E3 = 1, E5 = 0 and E6 = 0. A suitable inhibit signal E7 (waveform 23 of Fig. 10) is developed at the output of NAND gate Q7D (since E7 = (E3) (E5) (E6)).

At D4 the number transferred to the time-shared counter from the selected RAM address is examined. Consider a typical requirement for operation in the torque duration indication mode. If a conversion rate of 1·024 kHz is chosen and if a readout is to be advanced for each second of totalized time that the torque level falls within the torqueband for that readout, then when the stored pre-count reaches 1024, a pulse must be transferred to the readout. Under certain circumstances it is possible for the prescribed pre-count limit to be reached at a number of addresses within a short time of each other. However only one readout can be advanced at a time, hence it is desirable that over-range capability be provided. For the particular case cited the circuit has been arranged such that an output pulse will be generated each time a count state between 1024 and 4095 is detected. If, say, a state 4017 is detected then 1024 will be subtracted at the time the first output pulse is generated and so on until a state below 1024 is detected.

The prescribed number at or above which a readout pulse will be generated is set by the connection of the logic block (incorporating quad 2-input NOR gate Q16 and other components) which is interposed between two consecutive RAM inputs and two associated time-shared counter parallel outputs. Define as indicated in Figure 7:

X_1 as the more significant of the two outputs from the time-shared counter,
Y_1 as the less significant of the two outputs from the time-shared counter,
Z_1 as a control input,
X_2 as the more significant of the two RAM inputs,
Y_2 as the less significant of the two RAM inputs,
and Z_2 as a control output.

Further define:

n_1 as the number (0 to 3) formed by the X_1 and Y_1 counter outputs,
and n_2 as the number (0 to 3) formed by the X_2 and Y_2 RAM inputs.

The logic block is arranged such that if the control input Z_1 is 1 a straight transfer of the counter outputs to the RAM inputs will occur, and if Z_1 is 0 then n_2 will be 1 less than n_1 if $n_1 \geq 1$. With the logic block system used the RAM may hold up to $4N_P - 1$ (i.e. $3N_P - 1$ in excess of the prescribed limit N_P) before any information is lost. Logically the relationship between inputs and outputs of the logic block is as follows:

$$X_2 = X_1 (Y_1 + Z_1)$$

$$Y_2 = Y_1 Z_1 + X_1 (Y_1 + Z_1)'$$

$$Z_2 = Z_1 + (X_1 + Y_1)'$$

Hence the following truth table applies.

X_1	Y_1	Z_1	n_1	X_2	Y_2	Z_2	n_2
0	0	1	0	0	0	1	0
0	1	1	1	0	1	1	1
1	0	1	2	1	0	1	2
1	1	1	3	1	1	1	3
0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0
1	0	0	2	0	1	0	1
1	1	0	3	1	0	0	2

Control input Z_1 (waveform 24 of Fig. 7) is given logically by

$$Z_1 = \{(E7)\ D\}'$$

where E7 is the clock inhibit signal discussed above and D (waveform 4 of Fig. 9) is the HF CLK divide-by-8 output. Thus during the memory cycles for which a check is made to determine whether the stored number is equal to or greater than the prescribed limit (1024 for the special case considered) Z_1 will switch low as indicated in Figure 10. When such a number is detected Z_2 will switch low for the period Z_1 is low. In that case a pulse E8 (waveform 25 of Fig. 10) will be generated at D4 and transferred to flip flops Q19A and B. Q19B will not normally change state but its output state E9 (waveform 26 of Fig. 10) will be checked at this time to ensure E9 is 0. Q19A will change state as indicated via E10 (waveform 27 of Fig. 10). As a consequence the CLOCK ENABLE input to counter Q3 will be set high causing the count state in Q3 to be "frozen" (while E10 is high). While E9 is low and E10 high, OUTPUT ADDRESS DISABLE E11 (waveform 28 of Fig. 10) will switch low and the clocked address in decade counter Q3 will be transferred to the tri-state output bus resulting (Sec. 3.2.5) in the transfer of a pulse to the appropriate readout.

At D5 the time-shared counter reset function is inhibited.

At D6 a number reduced by 1024, for the link positions indicated in Figure 7, will be written into memory.

Normal read and write operations take place at D7 and D0 but no subtraction occurs.

At D1 (next memory cycle) E6 (waveform 22 of Fig. 10) will switch high. Multiplexer Q2 will now switch from the clocked address output of Q3 to address 13. Once again the multiplexer output will be enabled if the GATE is high and the LF CLK low. After a prescribed number of LF CLK cycles have passed, the time-shared counter output connected to terminal P5 will switch high causing the flip flop Q19B output E9 (waveform 26 of Fig. 10) to switch back high at D4. E9 remains high until the output at terminal P5 reverts again to the low state. The transition of E9 from the high to the low state causes the output E10 of flip flop Q19A to switch back to the low state.

A RESET GATE E12 (waveform 29 of Fig. 10) is generated at the output of NAND gate Q18C. Logically E12 = E10 + E6. At D4 the RESET GATE switches low and at D5 the contents of the time-shared counter are cleared.

At the commencement of the next memory cycle subsequent to E10 reverting to the low state, CONTROL GATE E6 will switch back high. Once again the clocked address will be selected via multiplexers Q2 and the whole sequence of searching for an address (0 to 9) containing a number equal to or higher than the prescribed limit will be repeated.

Enabling of the output address will occur for only half of the time that address 13 is selected. For a 1·024 kHz LF CLK frequency (set by link connection to P6) and for the particular connection to P5, shown dotted in Figure 7, an output pulse of $\frac{1}{8}$s duration will be generated but another pulse cannot be generated until at least another $\frac{1}{8}$s has elapsed. This feature prevents a count being missed because a readout receives two pulses in succession insufficiently spaced in time.

Alternative link connections allow the pre-counter division factor and the readout pulse duration to be varied over a wide range.

In the following table the pre-counter division factor N_P is given as a function of the link positions chosen.

Pre-counter Division Factor N_P	Required Link Connections*
1	P1 → P27, P2 → P29, P3 → P30, P4 → P28
2	P1 → P25, P2 → P27, P3 → P28, P4 → P26
4	P1 → P23, P2 → P25, P3 → P26, P4 → P24
8	P1 → P21, P2 → P23, P3 → P24, P4 → P22
16	P1 → P19, P2 → P21, P3 → P22, P4 → P20
32	P1 → P17, P2 → P19, P3 → P20, P4 → P18
64	P1 → P15, P2 → P17, P3 → P18, P4 → P16
128	P1 → P13, P2 → P15, P3 → P16, P4 → P14
256	P1 → P11, P2 → P13, P3 → P14, P4 → P12
512	P1 → P9, P2 → P11, P3 → P12, P4 → P10
1024	P1 → P7, P2 → P9, P3 → P10, P4 → P8

* Where the logic block is not interposed, direct connection between the time-shared counter outputs and the RAM inputs is required.

It is to be noted that the maximum division factor for the circuit drawn in Figure 7 is 1024. If a conversion rate of greater than 1·024 kHz were required to accommodate an input signal having wider bandwidth then either the readout rate could be increased above 1 pulse per second of totalized time or the RAM and time-shared counter could be extended. Hence two devices would provide an additional 2^4 division factor. Extension of the storage and counting range would not require any change in the programming circuits.

For convenience define the output pulse duration as T_0. The maximum number of pulses which can be transferred to the readouts per second is always less than $1/(2T_0)$. If we consider the maximum readout rate for a particular torqueband then the minimum pulse spacing will be given by the sum of:

(i) The duration T_0 of a readout pulse.

(ii) The duration T_0 of the interpulse gap.

(iii) The duration of 10 cycles of the LF CLK over which interval a search is made for an address (0 to 9) having a stored count equal to or greater than the prescribed pre-counter limit (a search always starts at the address one higher than that at which the previous output pulse was transferred).

Hence the maximum readout rate f_{mR} for a particular band is given by

$$f_{mR} = \frac{1}{2T_0 + 10/f_L} \text{ Hz}$$

For the torque duration indicator the maximum average readout rate is $1/(4T_0)$ Hz since $1/(2T_0)$ Hz is too fast, as indicated above, and the rate can only be varied by factors of 2. Thus the maximum duty cycle which can be applied to the readouts for the torque duration indicator is 25%.

For the level exceedance indicator the readout rate for a particular band can be increased to f_{mR} without data loss. If the readout is updated for each fatigue cycle counted then, in this instance, the maximum fatigue cycle rate or input signal frequency which can be handled is f_{mR}.

In the following table output pulse duration and maximum readout rate are given as a function of the link connection to terminal P5.

Duration (T_0) of Readout Pulse	Maximum Readout Rate f_{mR} $\left[f_{mR} = 1/(2T_0 + 10/f_L)\right]$	Terminal to be Linked to P5
$\frac{1}{f_L}$	$\frac{f_L}{12}$	P30
$\frac{2}{f_L}$	$\frac{f_L}{14}$	P28
$\frac{4}{f_L}$	$\frac{f_L}{18}$	P26
$\frac{8}{f_L}$	$\frac{f_L}{26}$	P24
$\frac{16}{f_L}$	$\frac{f_L}{42}$	P22
$\frac{32}{f_L}$	$\frac{f_L}{74}$	P20
$\frac{64}{f_L}$	$\frac{f_L}{138}$	P18
$\frac{128}{f_L}$	$\frac{f_L}{266}$	P16
$\frac{256}{f_L}$	$\frac{f_L}{522}$	P14
$\frac{512}{f_L}$	$\frac{f_L}{1034}$	P12
$\frac{1024}{f_L}$	$\frac{f_L}{2058}$	P10
$\frac{2048}{f_L}$	$\frac{f_L}{4106}$	P8

When the torque duration indication mode is used and an output is being generated on a particular band the individual repetition periods will not be all equal but there will be two possibilities differing by the duration of 10 cycles of the LF CLK. Consider the arrangement formed by the dotted link connections of Figure 8. In that instance:

LF CLK frequency $f_L = 1{\cdot}024$ kHz

Pre-counter division factor = 1024

Output pulse duration $T_0 = 128/f_L = 0{\cdot}125$ s

Hence on the average there will be one output pulse generated for each second of totalized time (average output pulse rate thus being equal to 1 Hz). In other words an output pulse will be generated on the average for every 1024 cycles of the LF CLK. For each output pulse generated no search of the stored counts will occur for the period of 256 cycles of the LF CLK (128 cycles will pass while the pulse is being generated and another 128 while the following separation gap is being generated). Thus, on the average, 768 (equal to 1024–256) cycles of the LF CLK will be generated while RAM addresses 0 to 9 are searched at the LF CLK rate for an address containing more than 1023 in storage. But a particular address will be examined only once every 10 cycles of the LF CLK. Hence the output pulse repetition period will be either the duration of 1016 (equal to 256 + 760) or 1026 (equal to 256 + 770) cycles of the LF CLK. To provide the average

repetition period equal to the duration of 1024 cycles of the LF CLK two periods out of ten will be equal to $1016/f_L$ and eight will be equal to $1026/f_L$. The 10-period average (a quantity which can be readily measured with many electronic counters) will remain constant at $1024/f_L$ (equal to 1 s).

Hence the predicted repetition periods consistent with the above analysis will be:

(i) For 2 cycles in 10 — 992188 μs

(ii) For 8 cycles in 10 — 1001953 μs

(iii) Average over 10 (or 5) cycles 1000000 μs

Measured values were almost in exact agreement with the predicted figures.

Obviously the electromechanical readouts limit the maximum number of output pulses which can be counted per second. For the type of readout chosen (Appendix I.5) the specified maximum counting rate is 25 Hz. However on units recently tested satisfactory operation with T_0 of $\frac{1}{64}$ s, and repetition frequency of about 30 Hz has been established. In establishing the maximum operating frequency the level exceedance mode of operation was chosen and the following settings were used:

(i) P6 was connected to P24 to provide an LF CLK rate of 8192 Hz (the maximum rate which can be used).

(ii) P1 was connected to P27, P2 to P29, P3 to P30 and P4 to P28 to provide a pre-counter division factor of unity (but still preserving the over-range capability).

(iii) P5 was connected to P16 to generate pulses of $\frac{1}{64}$ s duration for the readouts.

For the above settings the predicted maximum output pulse rate f_{mR} is give by

$$f_{mR} = \frac{1}{2T_0 + 10/f_L}$$

where $T_0 = \frac{1}{64}$ s and $f_L = 8192$ Hz. Substituting these values yields $f_{mR} = 30{\cdot}8$ Hz which agrees closely with the measured figures.

If an LF CLK rate of 1024 Hz were used (P6 connected to P18) and the output pulse duration were once again set to $\frac{1}{64}$ s (P5 connected to P22) then the maximum output pulse rate would be 24·4 Hz, a figure which was also confirmed by measurement.

For torque duration indication there are normally no special demands on output pulse transfer rate. However if improved time resolution were required this can be increased in binary steps from the 1 pulse per second of integrated time yielded by the link connections indicated in Figure 7 to 1 pulse for every $\frac{1}{16}$ s of integrated time. An LF CLK rate of 1024 Hz, a pre-counter division factor of 64, and an output pulse duration of $\frac{1}{64}$ s would yield the latter output rate.

Where maximum signal bandwidth is required a conversion rate (equal to LF CLK rate) of 8192 Hz can be used and a minimum of 8 pulses would be transferred to the readouts per second (for the pre-counter division factor having maximum value of 1024).

The START SYNC input (waveform 30 of Fig. 10) causes all RAM addresses accessed while the E3 GATE is high to be reset to the zero state via E14 (waveform 31 of Fig. 10). Since addresses 0 through 9 will be accessed in the clocked address mode of operation all pre-counter states will be zero at the trailing edge of the START SYNC pulse. One of the main advantages of the use of the START SYNC is that erroneous outputs on torquebands of high significance cannot occur at power switch-on.

The contents of RAM address 13 (allocated for output pulse generation) are not initially cleared so it is possible that the first readout pulse only may be missed. Thereafter RAM address 13 will be cleared following the generation of each output pulse.

Capacitors C6 and C7 (Fig. 7 and Appendix I.3) were found to be necessary for correct operation of the pre-counter circuit.

3.2.5 Start Synchronizing Signal Generator and Output Driver Circuit

Complete circuit and layout details on the start sync generator and output driver circuit are given in Figures 11 and 12 respectively. There are three separate functions performed by this circuit:

(i) Generation of a signal which resets various circuits at the time power is first applied and delays application of 28 VDC to the readouts.

(ii) Decoding the 4-line output address from the pre-counter to give a 10-line output suitable for driving the readouts.

(iii) Provision of buffering for some signals which are taken to an external connector for monitoring purposes.

To prevent erroneous counts being registered in the readouts at the time power (115 VAC) is first applied it is desirable that application of 28 VDC to the readouts be delayed somewhat to allow the regulated outputs ±15 V and +5 V to come up to specification. Further (as mentioned in Sec. 3.2.4) it is desirable that the pre-counter states for all bands be initially reset to zero so that there is no chance of an output pulse being transferred to a high torqueband readout at this time.

A delay circuit (Fig. 11) powered from the +5 V regulator output is used. Prior to the application of power, capacitor C3 will be discharged. When AC power is first applied the output of the +5 V regulator will rise towards its specified value and the output of comparator Q1 will switch to the high state. The comparator output is taken to input IN6 of tri-state hex buffer Q7. A buffered START SYNC output is obtained at output OUT6 which is permanently enabled.

After a delay period 0·7 (C3) (R1) second approximately (where C3 is expressed in microfarad and R1 in megohm) the output of comparator Q1 will revert to and be maintained thereafter at the low state. As a consequence the START SYNC output will switch low and relay K1 will be energized thus connecting 28 VDC to the readouts and their driving circuits. For the values of R1 and C3 indicated in Figure 11 the delay will be 0·3 second approximately.

The START SYNC output is used to initially clear certain circuits (Secs. 3.2.3 and 3.2.4) to ensure that no readout pulse is generated (after the initial delay period has elapsed) until a full interval of integrated time (torque duration indication) has been totalized or a complete fatigue cycle (level exceedance indication) has been counted.

The switched 28 VDC is taken to the EMC-H (electromechanical counter-high) output which is coupled to one side of all readout coils.

As indicated in Section 3.2.4 the output of the pre-counter comprises a 4-line BCD address (0 to 9 corresponding to readouts for bands 1 to 10 respectively) which is enabled when a readout coil is to be energized. The pre-counter output address is taken to address inputs OAD-1 to OAD-8 (Fig. 11).

Optical isolators Q2 to Q5 transfer the input address to the input of the BCD to decimal decoder Q6 without signal inversion. A high state is generated on the selected output of this decoder. Darlington transistor arrays Q9 and Q10 driven from the 10-line output from the decoder provide adequate current output for the readout coils. Typically the readout coils draw about 120 mA when energized.

Isolation of indicator circuit common and 28 VDC power common is achieved by the use of the optical isolators. Actually the indicator common is connected to chassis in the vicinity of the analogue amplifier input. Chassis is remotely connected, via the aircraft frame, to the negative side of the 28 VDC input. With this arrangement a single point grounding is achieved thus preventing the flow of ground loop currents through the indicator chassis. Output transistors and the decoder are powered from a nominal +5 V supply derived from the switched 28 VDC supply by Zener diode CR4 and associated components.

To facilitate the adjustment (Sec. 3.2.2) and checkout of the indicator the 8-line ADC output (Fig. 3) is buffered via Q7 and Q8 (refer to interwiring details in Appendix 2) and taken to output signal monitor connector J3. Ancillary display equipment coupled to that connector is used to provide an octal display (000 to 377 corresponding to 000 to 255 decimal) of the ADC output. Other signals HF CLK, LF CLK and OUTPUT GATE (also referred to as OUTPUT ADDRESS DISABLE E14 in Sec. 3.2.4) are similarly buffered whereas the START SYNC which originates as an output from buffer Q7 is taken directly to J3.

It has been found desirable to permanently ground the ENABLE input (Fig. 11) thus enabling the tri-state outputs of buffers Q7 and Q8 which carry the 8-bit ADC information. Because the conversion time is only about 4 μs negligible flicker results if the output is displayed directly even if the maximum conversion rate of 8192 Hz were selected. Some tests were successfully performed with the ENABLE input connected to the OUTPUT DISABLE (waveform 5 of Fig. 6) which switches low at the LF CLK rate for an interval of 8T (approximately 8 μs).

However since tri-state devices Q7 and Q8 draw more supply current when in the high impedance state it was considered best to permanently enable the tri-state outputs.

A listing of the signals to be coupled to the output signal monitor connector J3 (Appendix 2) is given below.

Signal Description	Output Buffer Designation (Fig. 11)
ADC Bit 1	BUF 1
ADC Bit 2	BUF 2
ADC Bit 3	BUF 3
ADC Bit 4	BUF 4
LF CLK	BUF 5
START SYNC	START SYNC
ADC Bit 5	BUF 7
ADC Bit 6	BUF 8
ADC Bit 7	BUF 9
ADC Bit 8	BUF 10
OUTPUT GATE	BUF 11
HF CLK	BUF 12

4. CALIBRATION AND TEST PROCEDURES

Calibration and test procedures for the Mk.2 system are similar to those adopted for the Mk.1 system[1].

For full scale calibration a dead weight pressure tester capable of providing calibration pressures in the range 0 to 150 psi adjustable in increments of not more than 1 psi is required.

Functional checking of the equipment using a tester (as for the Mk.1 system) which incorporates a series of resistors, which may be switched in turn across one arm of the strain gauge bridge (within the pressure transducer) is used.

To facilitate re-calibration and checkout of the Torque Spectrum Indicator a Signal Monitor (Fig. 13) is used. This item of ancillary test equipment, used for ground checking purposes only, is plugged directly into the output signal monitor socket J3 in the indicator. Displays Q1 to Q3 (Fig. 13) provide numerical indication of the ADC output in octal code and facilitate adjustment of the zero and gain potentiometers in the analogue amplifier at the time of calibration.

Power for the monitor is drawn from the indicator +5 V supply so that connection to an external power source becomes unnecessary. Current demand for the monitor is about 0·3 A.

For operational checking of the indicator, output signals HF CLK, LF CLK, OUTPUT GATE and START SYNC are brought out to readily accessible jacks on the front panel of the monitor.

5. PERFORMANCE OF COMPLETED CIRCUITS

The Torque Spectrum Indicator (Fig. 14) has been manufactured as a ruggedized unit which may be "hard" mounted in a helicopter or other vehicle. A set of three such indicators was fitted in a Sea King helicopter (operated by the RAN) in June 1978 and have been successfully acquiring torque data which will allow computations to be made on the safe fatigue life of critical gears. These indicators have been set for torque duration indication with the following parameter settings:

(i) Conversion rate of 1024 per second for each transducer channel.

(ii) Totalized time increments of 1 second for the electromechanical counters.

(iii) Electromechanical counter energizing pulse duration of 125 millisecond.

At the completion of each flight the readouts for the three indicators are photographed. Periodically the photographs are sent to these laboratories for analysis.

Operation of the indicators using all the available link options has been fully checked. Similarly all ancillary function testing and display equipment has been manufactured and fully tested.

As indicated in Section 3.2.4 the electromechanical impulse counters have been checked for operation at higher switching rates. Under laboratory conditions faultless operation has been demonstrated at 30 Hz rate using $\frac{1}{64}$ s pulses. Further testing would be required to establish whether the above pulse duration was adequate under more severe environmental conditions. If the 30 Hz rate can be accommodated then the present electromechanical impulse counters (Appendix 1.5), when used in a level exceedance indicator, would provide individual cycle counting according to the following specification:

(i) Maximum signal frequency for output on a single counter would be 30 Hz approximately.

(ii) Maximum signal frequency for output on all 10 counters would be 3 Hz approximately.

(iii) Transients equivalent to 3 cycles (traversing full range of the 10 counters) at up to about 100 Hz rate could be accommodated without data loss.

Similar counters (to those used for the above test) having a maximum counting rate of 50 Hz are available from the same manufacturer. Such counters could be used if wider signal bandwidth were required.

The specified counters are quite suitable for torque duration indication in Sea King helicopters. Similar counters used in the Mk.1 Analyser have demonstrated their reliability since their installation in 1975.

Each indicator requires 115 VAC 400 Hz single-phase and 28 VDC primary power supplies. Current demands are as tabulated below.

Supply	Current Demand
115 VAC	0·25 A
+28 VDC	30 mA (average), 135 mA (peak)

Measured current demands for regulated supplies internal to the indicator are given in the following table.

Supply	Current Demand
V_{AA} (+15 V)	70 mA (one transducer), 100 mA (two transducers)
V_{BB} (−15 V)	70 mA (one transducer), 100 mA (two transducers)
V_{CC} (+5 V)	1·45 A (indicator only), 1·75 A (with signal monitor connected)

6. SUMMARY OF EXPERIMENTAL RESULTS

a) A simple system of indicating either the totalized time that torque loading falls within each of a number of specified bands or the total number of times a certain pair of torque levels is traversed (i.e. fatigue cycles) is described.

b) Load sensing is via a single transducer and only two adjustments are necessary at the time of calibration.

c) Individual torqueband limits are set by a plug-in field programmable read-only-memory. Band limits may be varied in steps of about 0·4% of full torque range. Any system non-linearity can be allowed for in the read-only-memory program so that 0·4% overall linearity is guaranteed.

d) Totalizing of time that torque loading falls within each band is performed with the aid of an electronic pre-counter with typically 1 millisecond resolution. A single time-shared counter and random access memory performs the pre-counting function for all bands.

REFERENCES

1. Fraser K. F. and Krieser U. R. — Load Spectrum Measuring Equipment Part 1 Details of Mk.1 System Presently Used to Acquire Data in Wessex Mk.31B Helicopters. ARL, Mech. Eng. Note 371, August 1978.

2. British Aircraft Corporation Australia Pty. Ltd. — Introducing a New System of Aircraft Structure Fatigue Damage Evaluation—gives details of a system developed by the Aeronautical Research Laboratories of the Australian Department of Defence and the British Aircraft Corporation Australia Pty. Limited.

APPENDIX 1

Component Lists

The following tables list the components used in the circuits described in the text. Components have been given an identification label (or legend) consisting of a letter prefix followed by a number. The letter prefix identifies the class of component as indicated in the following table.

Class of Component	Letter Prefix
Resistor	R
Capacitor	C
Diode	CR
Integrated or hybrid circuit	Q
Test socket	TS
Power supply	PS
Electromechanical counter	EMC
Chassis mounted plug or socket	J
Transistor	TR
Crystal	XL
Relay	K
Card extractor handle	CEH

The number following the letter prefix identifies the particular component of the specified class.

Resistance and capacitance values given in the component lists (and also marked on the circuit diagrams) are given respectively in units of ohm and picofarad (where $K = 10^3$ and $M = 10^6$ multiplication factors). Thus a capacitance value designated 10 K means 10 000 picofarad and a capacitance designated 6·8 M means $6{\cdot}8 \times 10^6$ picofarad or 6·8 microfarad.

1.1 Components for Board A (Analogue Amplifier and Transducer Excitation Generator)

Legend	Value	Description
R1	500	Resistor, variable, Vishay Type 1202P.
R2	680	Resistor, fixed, metal on glass, Vishay Type S102, ±1 PPM/°C, 0·1%.
R3		Use shorting link for present application.
R4	2 K	As for R2
R5		Use shorting link for present application.
R6	5·6	Resistor, fixed, wirewound, Welwyn Type W21, 2·5 watt
R7	560	Resistor, fixed, metal glaze, IRH Type RN1/4, 0·25 watt, ±25 PPM/°C, 1%.
R8	100	As for R7
R9	1 K	As for R1
R10	4·3 K	As for R2
R11		Use shorting link for present application.
R12	2·4 K	As for R7

1.1 Components for Board (Continued)

Legend	Value	Description
C15	33	As for C3
C16	100 K	As for C2
C17	1 M	As for C2, ±10%
C18	1 M	As for C2, ±10%
C19	1 M	As for C2, ±10%
C20		Select value on test to give 3·6 M ±5% total capacitance.
C21	330 K	As for C2, ±10%
C22		Select value on test to give 400 K ±5% total capacitance.
C23	330 K	As for C2, ±10%
C24		Select value on test to give 400 K ±5% total capacitance.
C25	100 K	As for C2
C26	33	As for C3
C27	100 K	As for C2
C28	100 K	As for C2
C29	100 K	As for C2
Q1		Integrated circuit, voltage regulator, LM723C, 14 pin DIL, NS
Q2		Integrated circuit, operational amplifier, LM308AH, 8 pin TO5, NS
Q3		Integrated circuit, precision instrumentation amplifier, AD521K, 14 pin DIL, Analog Devices
Q4		As for Q3
Q5		As for Q2
Q6		As for Q2
TR1		Transistor, silicon, NPN, 2N2219A, mount on heatsink—Thermalloy 2212B (for TO5 can)
TR2		Transistor, silicon, PNP, 2N3502, mount on heatsink—Thermalloy 2212B
L1	27	Inductor, 27 microhenry, Cambion type 2590/30
TS1		Test socket, white, Amp Part No. 3–582118–9
TS2		Test socket, white, Amp Part No. 3–582118–9
TS3		Test socket, green, Amp Part No. 3–582118–5
TS4		Test socket, yellow, Amp Part No. 3–582118–4
TS5		Test socket, black, Amp Part No. 3–582118–0
TS6		Test socket, blue, Amp Part No. 3–582118–6
TS7		Test socket, red, Amp Part. No. 3–582118–2
CEH		Printed circuit board extractor handle, EECO (Electronic Engineering Company) type H903

1.2 Components for Board B (Band Separator)

Legend	Value	Description
R1	100	Resistor, variable, 22 turn, wire wound, Bourns Model 3057P, only required for bipolar operation
R2	470	Resistor, fixed, metal glaze, IRH Type RN1/4, 0·25 watt
R3	470	As for R2
R4	470	As for R2
R5	470	As for R2
R6	470	As for R2
C1	100 K	Capacitor, fixed, phenolic dipped ceramic, Vitamron VK33BW series
C2	100 K	As for C1
C3	6·8 M	Capacitor, fixed, electrolytic, tantalum, Sprague Type 196D, 35 VW
C4	100 K	As for C1
C5	100 K	As for C1
C6	100 K	As for C1
C7	100 K	As for C1
C8	100 K	As for C1
C9	100 K	As for C1
C10	470	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW series
C11	44	Capacitor, variable, 4 to 44pF, Philips 2222–809–07008
C12		If necessary add fixed capacitor from Vitramon VK24BA or VK23BW series to obtain requisite output frequency.
C13	470	As for C8
C14	470	As for C8
XL1		Crystal, 2·097152 MHz, HY-Q coding CDX, mounted in can type D, mount in August socket assembly Class 525 Part No. 8000–AG36
Q1		Analog to digital converter, 8-bit, Datel Model EH8B
Q2		Integrated circuit, quad 2-input NOR gate, SN7402N, 14DIL
Q3		Integrated circuit, quad 2-input NAND gate, SN7400N, 14DIL
Q4		Integrated circuit, hex inverter, SN7404N, 14DIL
Q5		Integrated circuit, quad 2-input AND gate, SN7408N, 14DIL
Q6		Integrated circuit, hex inverter, SN7404N, 14DIL
Q7		Integrated circuit, 4-bit magnitude comparator, SN7485N, NS, 16DIL
Q8		Integrated circuit, 4-bit magnitude comparator, SN7485N, NS, 16DIL
Q9		Integrated circuit, 256 bit ROM, DM8578N, NS, (alternatively 82S123, Signetics), 16DIL, mount in socket.
Q10		Integrated circuit, 4-bit binary counter, SN7493N, 14DIL
Q11		Integrated circuit, dual 2: 4 demultiplexer, SN74155N, 16DIL
Q12		Integrated circuit, quad 2-input OR gate, SN7432N, 14DIL
Q13		Integrated circuit, tri-state programmable binary counter, DM8556N, NS, 16DIL
Q14		Integrated circuit, 16-bit RAM, SN7489N, 16DIL
Q15		Integrated circuit, dual D flip flop, SN7474N, 14DIL
Q16		Integrated circuit, quad 2-input OR gate, SN7432N, 14DIL
CEH		Printed circuit board extractor handle, EECO type H903.

1.3 Components for Board C (Pre-counter)

Legend	Value	Description
R1	470	Resistor, fixed, metal glaze, IRH Type RN1/4, 0·25 watt
C1	6·8 M	Capacitor, fixed, electrolytic, tantalum, Sprague Type 196D, 35VW
C2 →C8	100 K	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK33BW series
C9	1·5 K	As for C2
C10	470	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK23BW series
C11	150	As for C10
C12	470	As for C10
Q1		Integrated circuit, tri-state quad buffer, DM8094, NS, 14DIL
Q2		Integrated circuit, tri-state quad 2-input multiplexer, DM8123, NS, 16DIL
Q3		Integrated circuit, tri-state programmable decade counter, DM8555, NS, 16DIL
Q4		Integrated circuit, quad 2-input OR gate, SN7432N, 14DIL
Q5		Integrated circuit, 64-bit RAM, SN7489N, 16DIL
Q6		Integrated circuit, up-down binary counter, SN74193N, 16DIL
Q7		Integrated circuit, quad 2-input AND gate, SN7408N, 14DIL
Q8		Integrated circuit, triple 3-input NAND gate, SN7410N, 14DIL
Q9		Integrated circuit, 64-bit RAM, SN7489N, 16DIL
Q10		Integrated circuit, up-down binary counter, SN74193N, 16DIL
Q11		Integrated circuit, hex inverter, SN7404N, 14DIL
Q12		Integrated circuit, 64-bit RAM, SN7489N, 16DIL
Q13		Integrated circuit, up-down binary counter, SN74193N, 16DIL
Q14		Integrated circuit, quad 2-input NOR gate, SN7402N, 14DIL
Q15		Integrated circuit, quad 2-input AND gate, SN7408N, 14DIL
Q16		Integrated circuit, quad 2-input OR gate, SN7432N, 14DIL
Q17		Integrated circuit, quad 2-input OR gate, SN7432N, 14DIL
Q18		Integrated circuit, quad 2-input NAND gate, SN7400N, 14DIL
Q19		Integrated circuit, dual D flip flop, SN7474N, 14DIL
Q20		Integrated circuit, triple 3-input AND gate, SN7411N, 14DIL
Q21		Integrated circuit, dual D flip flop, SN7474N, 14DIL
Q22		Integrated circuit, 4-bit binary counter, SN7493N, 14DIL
Q23		Integrated circuit, BCD to decimal decoder, SN7442N, 16DIL
CEH		Printed circuit board extractor handle, EECO type H903

1.4 Components for Board D (Start SYNC Generator and Output Driver Circuits)

Legend	Value	Description
R1	100 K	Resistor, fixed, metal glaze, IRH Type RN1/4, 0·25 watt
R2	10 K	As for R1
R3	10 K	As for R1
R4	4·7 K	As for R1
R5	10	Resistor, fixed, Electrosil Type C5, glass-tin-oxide, 0·5 watt
R6	2 K	As for R1
R7	330	As for R1
R8	330	As for R1
R9	330	As for R1
R10	330	As for R1
R11	4·7 K	As for R1
R12	4·7 K	As for R1
R13	4·7 K	As for R1
R14	4·7 K	As for R1
C1	6·8 M	Capacitor, fixed, electrolytic, tantalum, Sprague type 196D, 35 VW
C2	100 K	Capacitor, fixed, phenolic dipped ceramic, Vitramon VK33BW series
C3	4·7 M	Capacitor, fixed, electrolytic, tantalum, Sprague type CS13B, 35 VW
C4	47 M	As for C4
C5	100 K	As for C2
C6	6·8 M	As for C1
CR1		Diode, silicon, OA202, Philips, 300 mA, 150 PIV
CR2		Diode, silicon, 1N4007, 1A, 1000 PIV
CR3		As for CR1
CR4		Diode, zener, 5·1V, BZX–79–5 V1, 400 mW
Q1		Integrated circuit, voltage comparator, LM311N, NS
Q2		Integrated circuit, optical isolator, Hewlett Packard 5082–4350, 8 DIL
Q3		Integrated circuit, optical isolator, Hewlett Packard 5082–4350, 8 DIL
Q4		Integrated circuit, optical isolator, Hewlett Packard 5082–4350, 8 DIL
Q5		Integrated circuit, optical isolator, Hewlett Packard 5082–4350, 8 DIL
Q6		Integrated circuit, BCD to decimal decoder (CMOS), CD4028C, NS, 16DIL
Q7		Integrated circuit, tri-state hex buffer, DM8097N, NS, 16 DIL
Q8		Integrated circuit, tri-state hex buffer, DM8097N, NS, 16 DIL
Q9		Darlington transistor array, 7 channel (5 only used), Sprague ULN-2003A, 16DIL
Q10		Darlington transistor array, 7 channel (5 only used), Sprague ULN-2003A, 16DIL
K		Relay, Magnecraft W118 DIP-1 (or Electrol 30381051), 14DIL
CEH		Printed circuit board extractor handle, EECO type H903

1.5 Components for Mainframe

Legend	Description
EMC-1 →EMC-10	Electromechanical impulse counter, 8 decade, 24VDC, 210 ohm coil, Hengstler 0–405–265 with socket
PS1	Power supply, AC to DC converter, +15 V and −15 V regulated outputs, 200 mA, Semiconductor Circuits Inc., Type SP5920 with options FB, K2, M, OV and T.
PS2	Power supply, AC to DC converter, +5 V regulated output, 2A, Semiconductor Circuits Inc., Type SP5941 with options FB, K2, M, OV and T.
J1	Plug, chassis mounting, 6 pin, Cannon KPT00A10-6P
J2	Socket, chassis mounting, 10 pin, Cannon KPT00A12-10S
J3	Socket, chassis mounting, 19 pin, Cannon KPT00A14-19S
J4 → J7	Socket, printed circuit edge type, solder tab, floating eyelet, 44 pin (22 per side), 0·156 inch pin spacing, Cannon G01.D44.B2AAKG

APPENDIX 2

Interwiring Details

Details of all interwiring within the Mk.2 Torque Spectrum Indicator are given in this section. The types of cable specified in the following table are used for the interwiring.

Legend	Description
W1	Cable, twisted pair shielded and jacketed, Raychem type 44A1121-9/0-9
W2	Cable, hook-up, multi-stranded, Ascand 7/0·010, black PVC insulation
W3	As for W2, but with red insulation
W4	As for W2, but with violet insulation
W5	As for W2, but with orange insulation
W6	As for W2, but with yellow insulation
W7	As for W2, but with blue insulation
W8	Cable, hook-up, multi-stranded, Ascand 5/0·0076, white insulation
W9	Cable, hook-up, single strand, 30 gauge, Kynar, white insulation
W10	Cable, shielded and jacketed, Raychem type 44A111-26-.

A summary of the connectors together with their application is given in the following table. Details on the types of connectors (referred to in this section) are given in Appendix 1.5.

Connector	Location	Application
J1	Rear Panel	Aircraft input power (115VAC and 28VDC) connector
J2	Rear Panel	Transducer input/output connector
J3	Rear Panel	Output signal monitor connector
J4	Internal Chassis	Board A (Analogue Amplifier and Transducer Excitation) edge connector
J5	Internal Chassis	Board B (Band Separator) edge connector
J6	Internal Chassis	Board C (Pre-counter) edge connector
J7	Internal Chassis	Board D (Start Sync Generator and Output Driver Circuits) edge connector.

Wiring to Regulated Power Supplies—PS1 (±15 V) and PS2 (+5 V)

Pin	Connected to	Signal Description	Wire Type
PS1–1	J1–C	115 VAC INPUT	W6
–2	J1–D	115 VAC RETURN	W2
–3	J5–T	V_{AA} (+15 V) OUTPUT	W5
–4	J5–6	ANALOG COM(0V)	W2
–5	J5–R	V_{BB} (−15 V) OUTPUT	W4
PS2–1	PS1–1	115 VAC INPUT	W6
–2	PS1–2	115 VAC RETURN	W2
–3	J7–B	V_{CC} (+5 V) OUTPUT	W3
–4	J7–1, J3–M	DIG COM	W2

Wiring to J1

(Power Input)

Pin	Connected to	Signal Description	Wire Type
A	J7–J	+28 VDC	W3
B	J7–K	28 VDC RETURN (to Aircraft Gnd)	W2
C	PS1–1	115 VAC	W6
D	PS1–2	115 VAC RETURN (to Aircraft Gnd)	W2
E	J3–N	LF CLK	W8
F	J3–M	DIG COM	W2

Wiring to J2

(Transducer Input/Output)

Pin	Connected to	Signal Description	Wire Type
A	J4–21	Shield Input A	W1—Shd (1)
B	J4–4	−Input A	W1—Black (1)
C	J4–Y	+5 V Excitation	W6
D	J4–3	+ Input B	W1—White (2)
E	J4–22	Shield Input B	W1—Shd (2)
F	J4–2	−Input B	W1—Black (2)
G	J4–17	−5 V Excitation	W7
H	J4–5	+ Input A	W1—White (1)
J	J4–U	+5 V Excitation Sense	W8
K	J4–18	−5 V Excitation Sense	W8

Wiring to J3

(Output Signal Monitor)

Pin	Connected to	Signal Description	Wire Type
A	J7–F	ADC Bit 1 (MSB)	W8
B	J7–E	ADC Bit 2	W8
C	J7–5	ADC Bit 3	W8
D	J7–C	ADC Bit 4	W8
E	J7–P	ADC Bit 5	W8
F	J7–N	ADC Bit 6	W8
G	J7–12	ADC Bit 7	W8
H	J7–10	ADC Bit 8	W8
J			
K			
L			
M	PS2–4, J1–F	COM	W2
N	J7–A, J1–E	LF CLK	W10*
P			
R			
S	J7–11	OUTPUT GATE	W8
T	J7–D	START SYNC	W8
U	PS2–3	+5 V	W3
V	J7–8	HF CLK	W10*

* Shields connected to J3–M at one end and left open at the other.

Wiring to J4

(Printed Circuit Board A—Analogue Amplifier and Transducer Excitation Generator)

Pin	Connected to	Signal Description	Wire Type
T	J5–T	V_{AA} (+15 V)	W5
6	J5–6	ANALOG PWR COM	W2
R	J5–R	V_{BB} (−15 V)	W4
5	J2–H	+ Input A	W1—white (1)
4	J2–B	− Input A	W1—black (1)
3	J2–D	+ Input B	W1—white (2)
2	J2–F	− Input B	W1—black (2)
Y	J2–C	V_{RP} (+ 5V TDR EXCIT)	W8
U	J2–J	V_{RP} SENSE	W8
21	J2–A	OUTPUT COM (Shd. IP A)	W1—Shd (1)
22	J2–E	OUTPUT COM (Shd. IP B)	W1—Shd (2)
A	J5–4	OUTPUT COM	W2
W	J5–3	ANALOG OUTPUT	W9
18	J2–K	V_{RN} SENSE	W8
17	J2–G	V_{RN} (−5 V TDR EXCIT)	W7

Wiring to J5

(Printed Circuit Board B—Band Separator)

Pin	Connected to	Signal Description	Wire Type
1, A	J6–1, J5–22	DIG COM	W2
B	J6–B	V_{CC} (+5 V)	W3
T	PS1–3, J4–T	V_{AA} (+15 V)	W5
6	PS1–4, J4–6	ANALOG COM	W2
R	PS1–5, J4–R	V_{BB} (−15 V)	W4
3	J4–W	ANALOG INPUT	W9
4	J4–A	INPUT COM	W9
8	J6–18	LF CLK	W9
F	J6–19	GATE	W9
17	J6–6	AD–8	W9
18	J6–7	AD–4	W9
20	J6–H	AD–2	W9
Y	J6–10	AD–1	W9
S	J7–L	Bit 8	W9
16	J7–M	Bit 7	W9
P	J7–13	Bit 6	W9
13	J7–Z	Bit 5	W9
11	J7–2	Bit 4	W9
10	J7–4	Bit 3	W9
L	J7–6	Bit 2	W9
H	J7–7	Bit 1	W9
12	J6–20	START SYNC	W9
M	J6–U	HF CLK	W9
19	No connection	OUTPUT DISABLE	
22	Chassis Term.	Chassis Ground Connection	W2

Wiring to J6

(Printed Circuit Board C—Pre-Counter)

Pin	Connected to	Signal Description	Wire Type
1, A	J7–1, J5–A, J6–22	DIG COM	W2
B	J7–B, J5–B	V_{CC} (+5 V)	W3
U	J7–H, J5–M	HF CLK	W9
20	J7–D, J5–12	START SYNC	W9
T	J7–9	OUTPUT GATE	W9
6	J5–17	AD–8	W9
7	J5–18	AD–4	W9
H	J5–20	AD–2	W9
10	J5–Y	AD–1	W9
12	J7–14	OAD–1	W9
13	J7–17	OAD–2	W9
S	J7–16	OAD–4	W9
P	J7–15	OAD–8	W9
18	J7–3, J5–8	LF CLK	W9
19	J5–F	GATE	W9
22	J6–1	DIG COM	W2

Wiring to J7

(Printed Circuit Board D—Start Sync Generator and Output Driver Circuits)

Pin	Connected to	Signal Description	Wire Type
1	PS2–4, J6–A, J3–M	DIG COM	W2
B	PS2–3, J6–B	V_{cc} (+5 V)	W3
J	J1–A	+28 VDC	W3
K	J1–B	28 VDC RETURN	W2
15	J6–P	OP Address 8	W9
16	J6–S	OP Address 4	W9
17	J6–13	OP Address 2	W9
14	J6–12	OP Address 1	W9
3	J6–18	LF CLK	W9
2	J5–11	ADC Bit 4	W9
4	J5–10	ADC Bit 3	W9
6	J5–L	ADC Bit 2	W9
7	J5–H	ADC Bit 1	W9
D	J6–20, J3–T	START SYNC	W9, W8
A	J3–N	Buf. LF CLK	W8
C	J3–D	Buf. Bit 4	W8
5	J3–C	Buf. Bit 3	W8
E	J3–B	Buf. Bit 2	W8
F	J3–A	Buf. Bit 1	W8
S	J7–1	DIG COM	W2
P	J3–E	Buf. Bit 5	W8
N	J3–F	Buf. Bit 6	W8
12	J3–G	Buf. Bit 7	W8
10	J3–H	Buf. Bit 8	W8
11	J3–S	Buf. OUTPUT GATE	W8
8	J3–V	Buf. HF CLK	W8
Z	J5–13	ADC Bit 5	W9
13	J5–P	ADC Bit 6	W9
M	J5–16	ADC Bit 7	W9
L	J5–S	ADC Bit 8	W9
9	J6–T	OUTPUT GATE	W9
H	J6–U	HF CLK	W9
T	"High" Side of all Electromech Count.	EMC–H	W6
U	"Low" EMC–10	EMC–10L	W8
18	"Low" EMC–9	EMC–9L	W8
V	"Low" EMC–8	EMC–8L	W8
19	"Low" EMC–7	EMC–7L	W8
W	"Low" EMC–6	EMC–6L	W8
22	"Low" EMC–5	EMC–5L	W8
Y	"Low" EMC–4	EMC–4L	W8
21	"Low" EMC–3	EMC–3L	W8
X	"Low" EMC–2	EMC–2L	W8
20	"Low" EMC–1	EMC–1L	W8

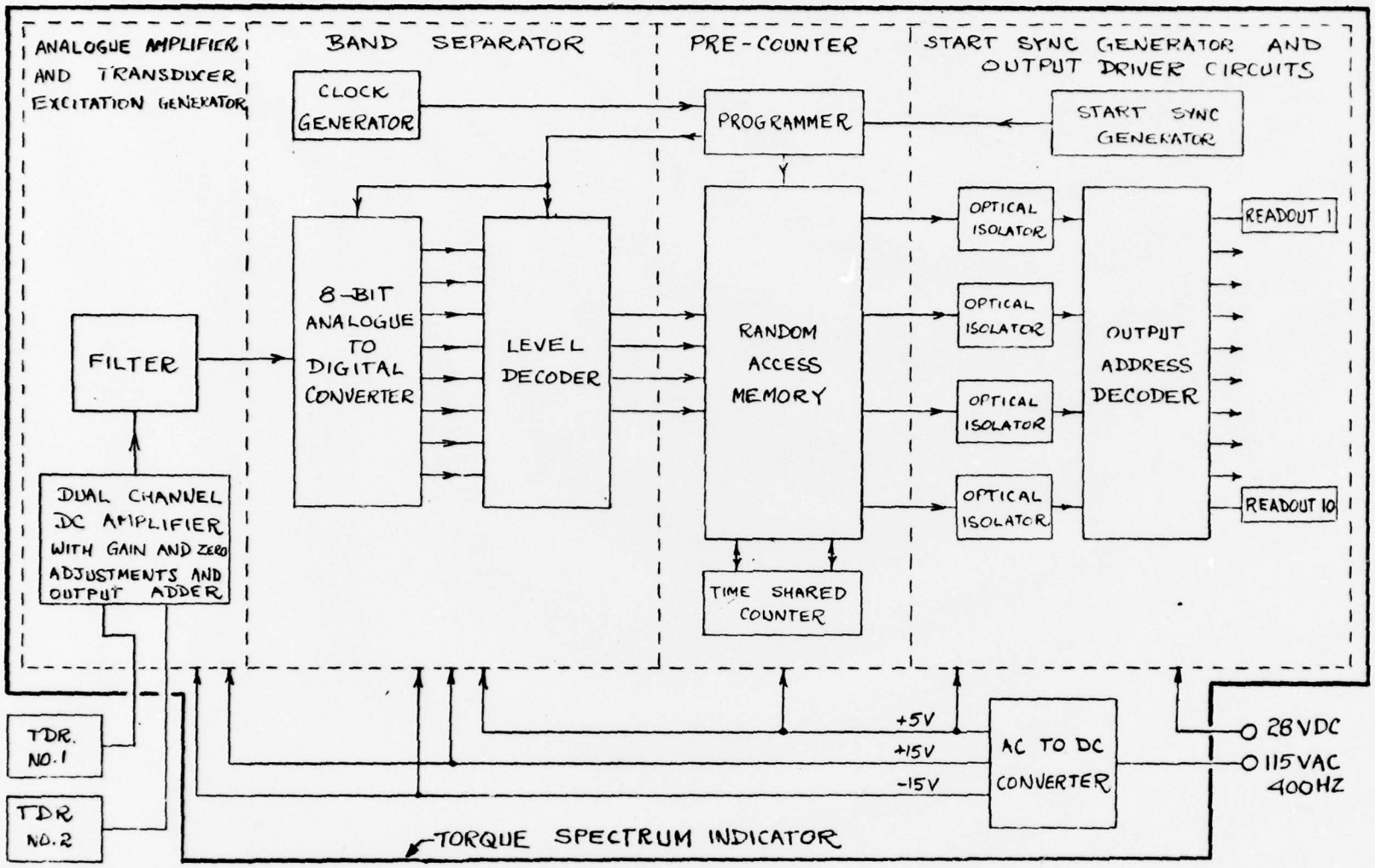


FIG. 1 BLOCK SCHEMA OF TORQUE LOAD INDICATING SYSTEM

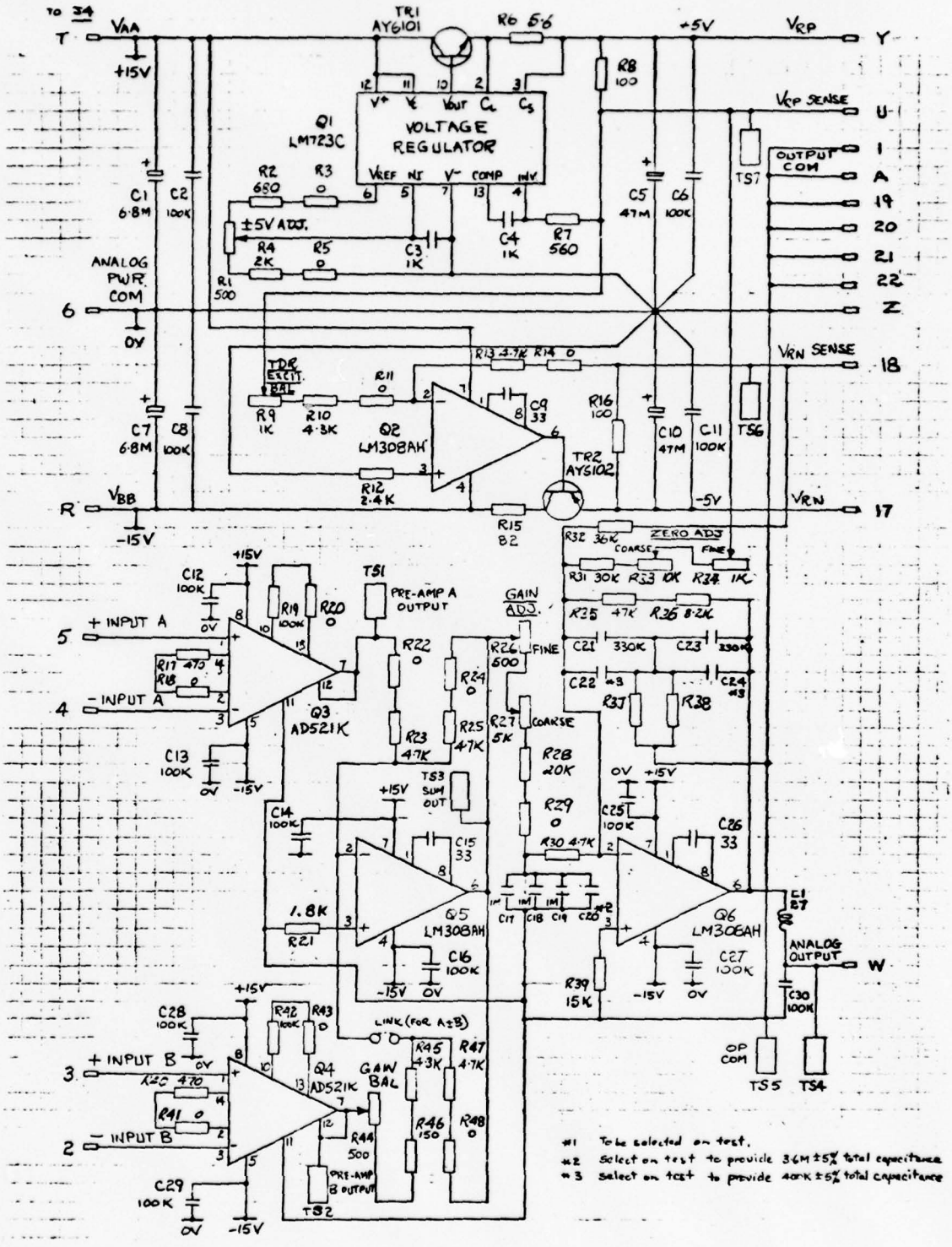


FIG. 2 ANALOGUE AMPLIFIER AND TRANSDUCER EXCITATION GENERATOR

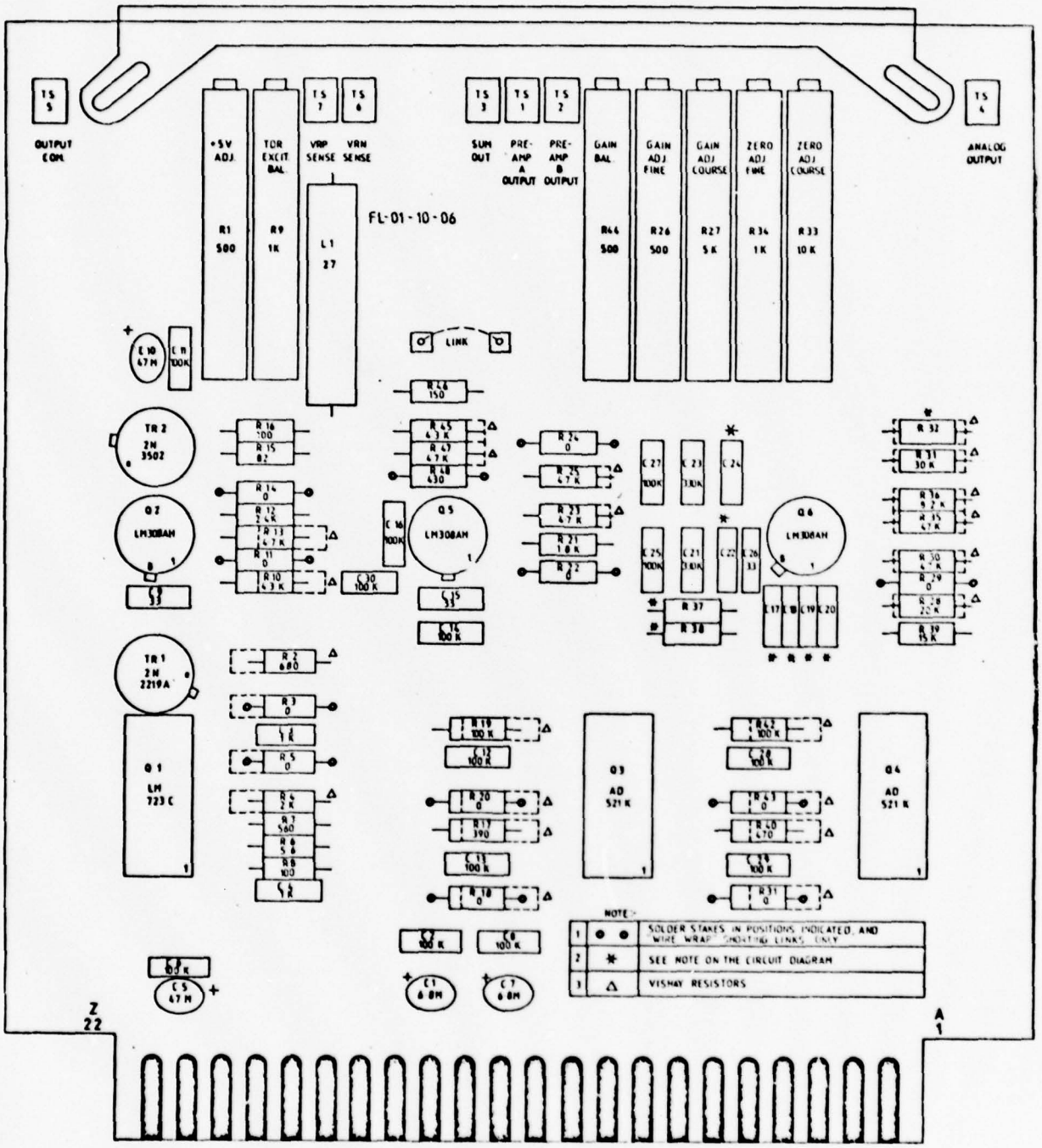
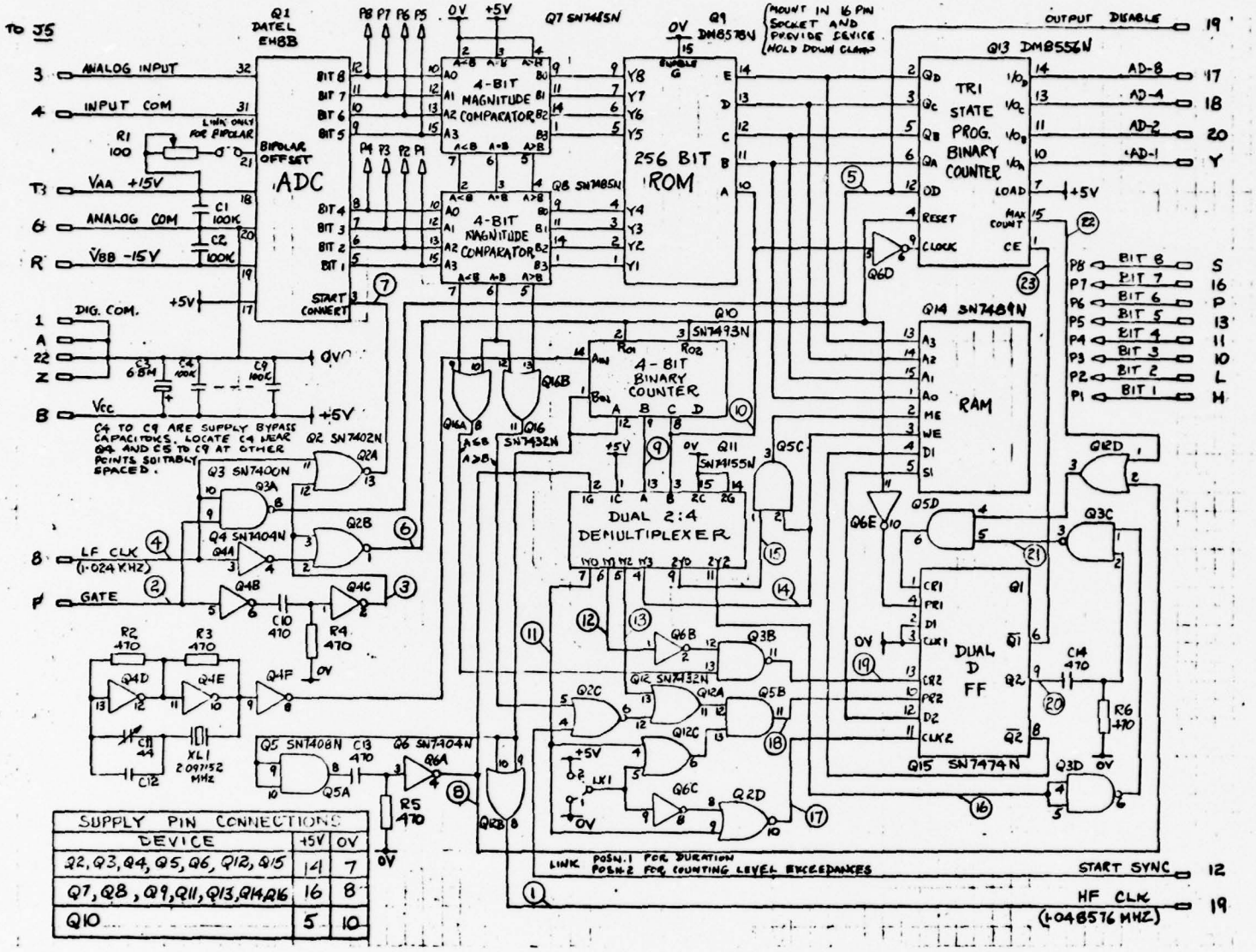


FIG. 3 COMPONENT LAYOUT FOR ANALOGUE AMPLIFIER AND TRANSDUCER EXCITATION GENERATOR



SUPPLY PIN CONNECTIONS		
DEVICE	+5V	0V
Q2, Q3, Q4, Q5, Q6, Q12, Q15	14	7
Q7, Q8, Q9, Q11, Q13, Q14, Q16	16	8
Q10	5	10

FIG. 4 **BAND SEPARATOR**

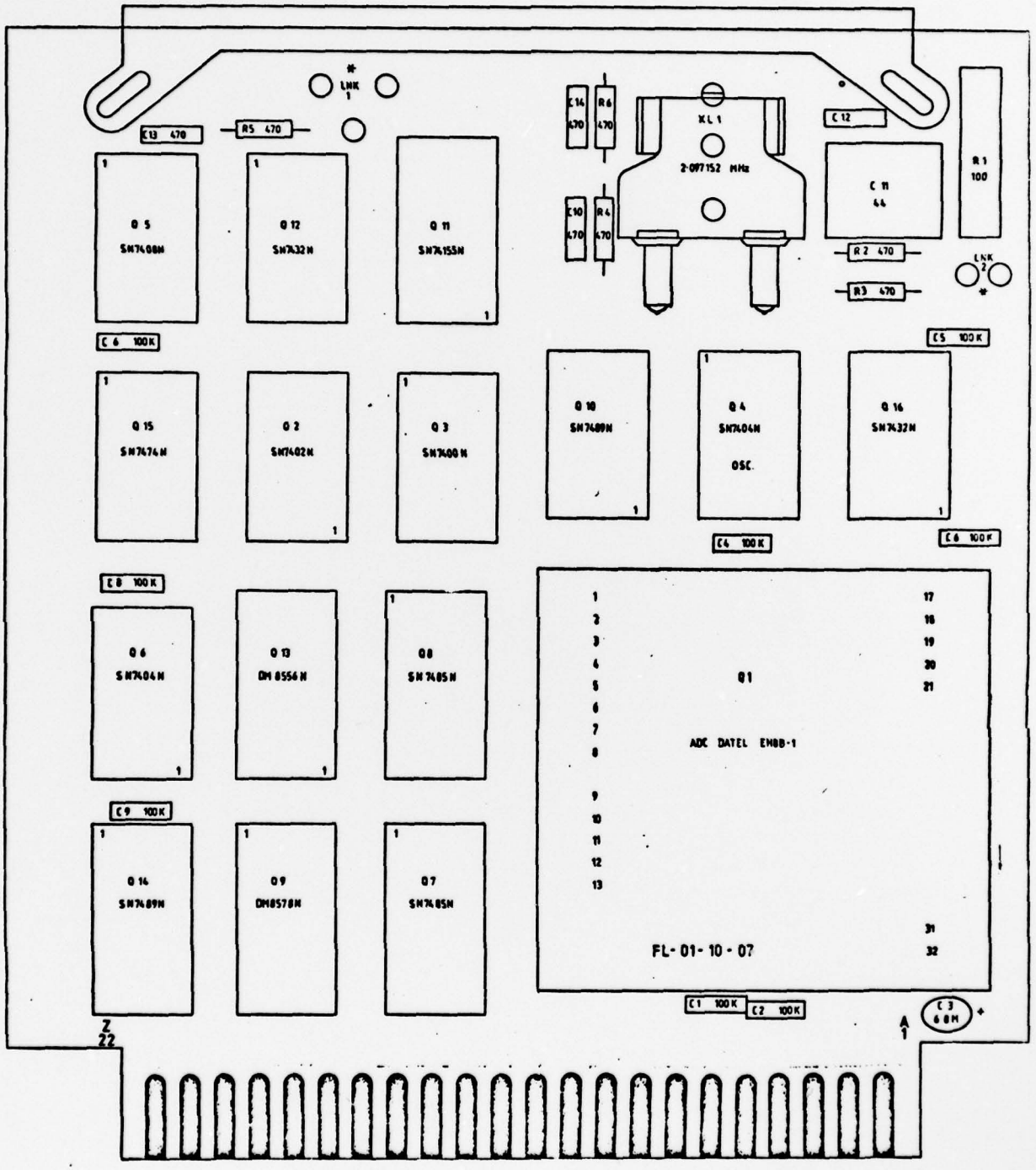
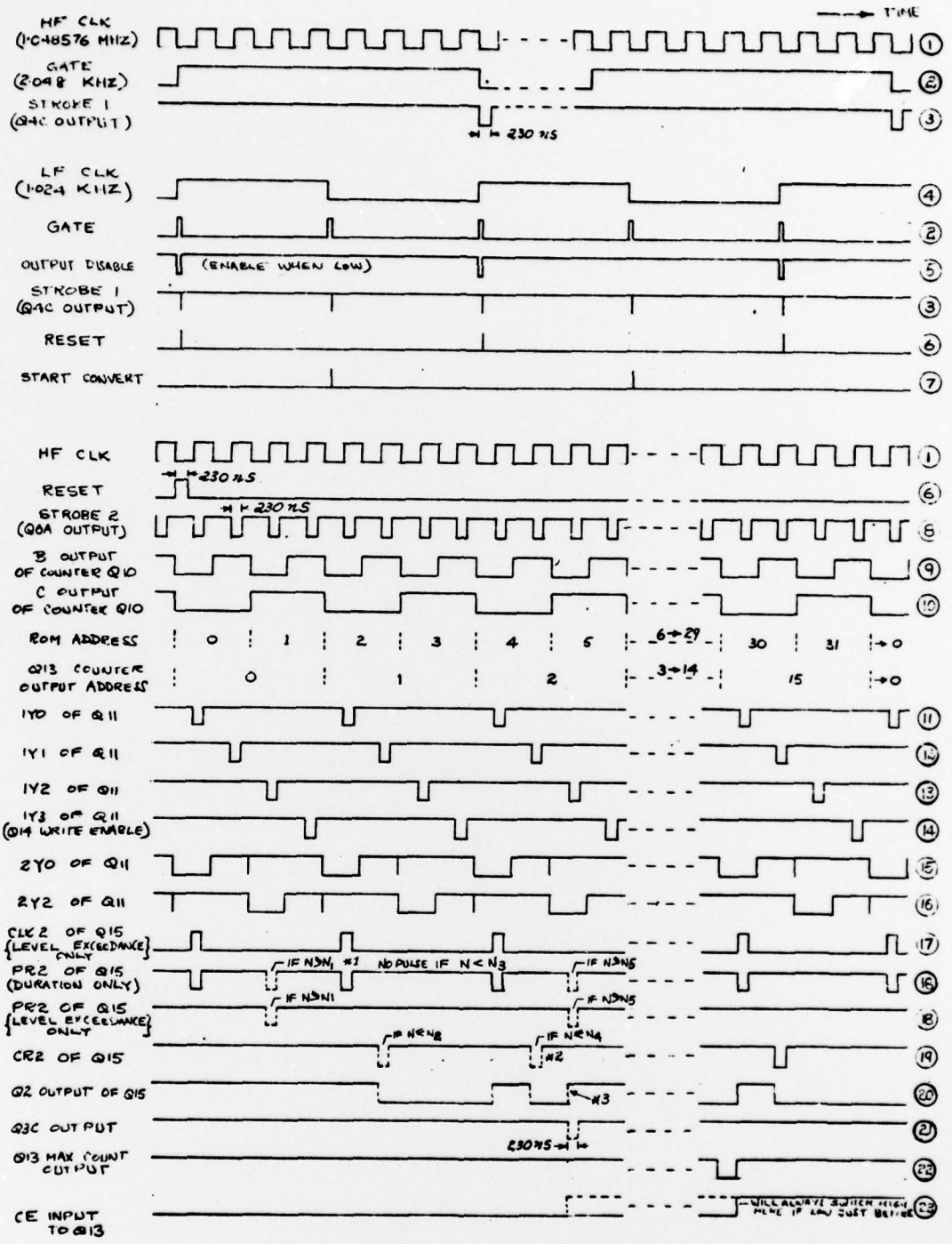


FIG. 5 COMPONENT LAYOUT FOR BAND SEPARATOR



#1 N=ADC OUTPUT NUMBER, N_3 = NUMBER STORED AT ADDRESS 3 OF ROM ETC.

#2 FOR 'LEVEL EXCEEDANCE' ROM IS PROGRAMMED SUCH THAT $N \geq N_5$ AND $N < N_4$ CAN NEVER OCCUR TOGETHER (AND SIMILARLY FOR ANY OTHER PAIR OF ADDRESSES)

#3 OCCURS IF $N_4 \geq N \geq N_5$ FOR 'TORQUE DURATION'
OCCURS IF $N \geq N_4$ APPLIED FOR PREVIOUS READINGS AND $N \leq N_4$ APPLIES FOR THIS READING FOR 'LEVEL EXCEEDANCE' ONLY.

FIG. 6 WAVEFORMS FOR BAND SEPARATOR

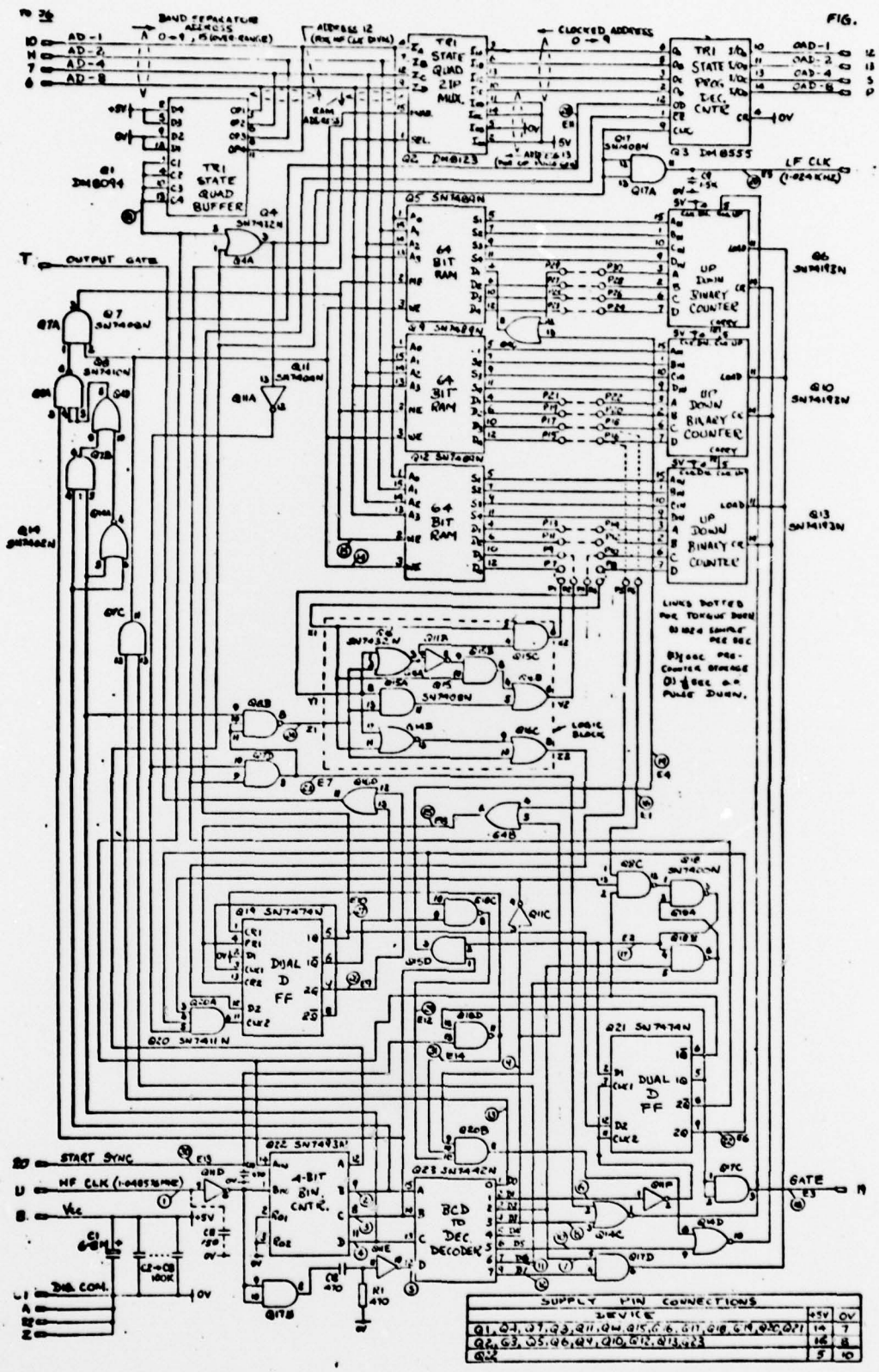


FIG. 7 PRE-COUNTER

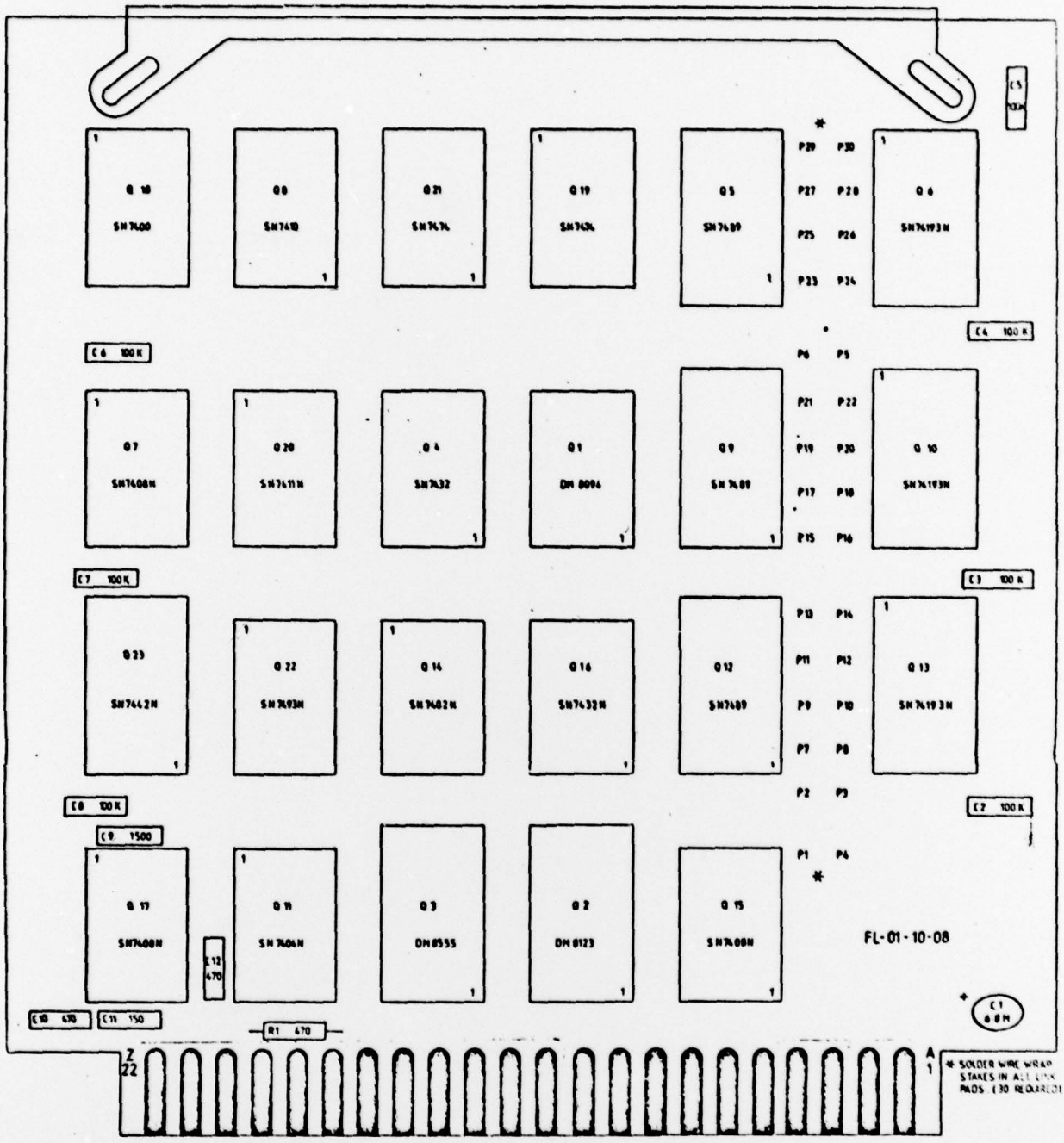


FIG. 8 COMPONENT LAYOUT FOR PRE COUNTER

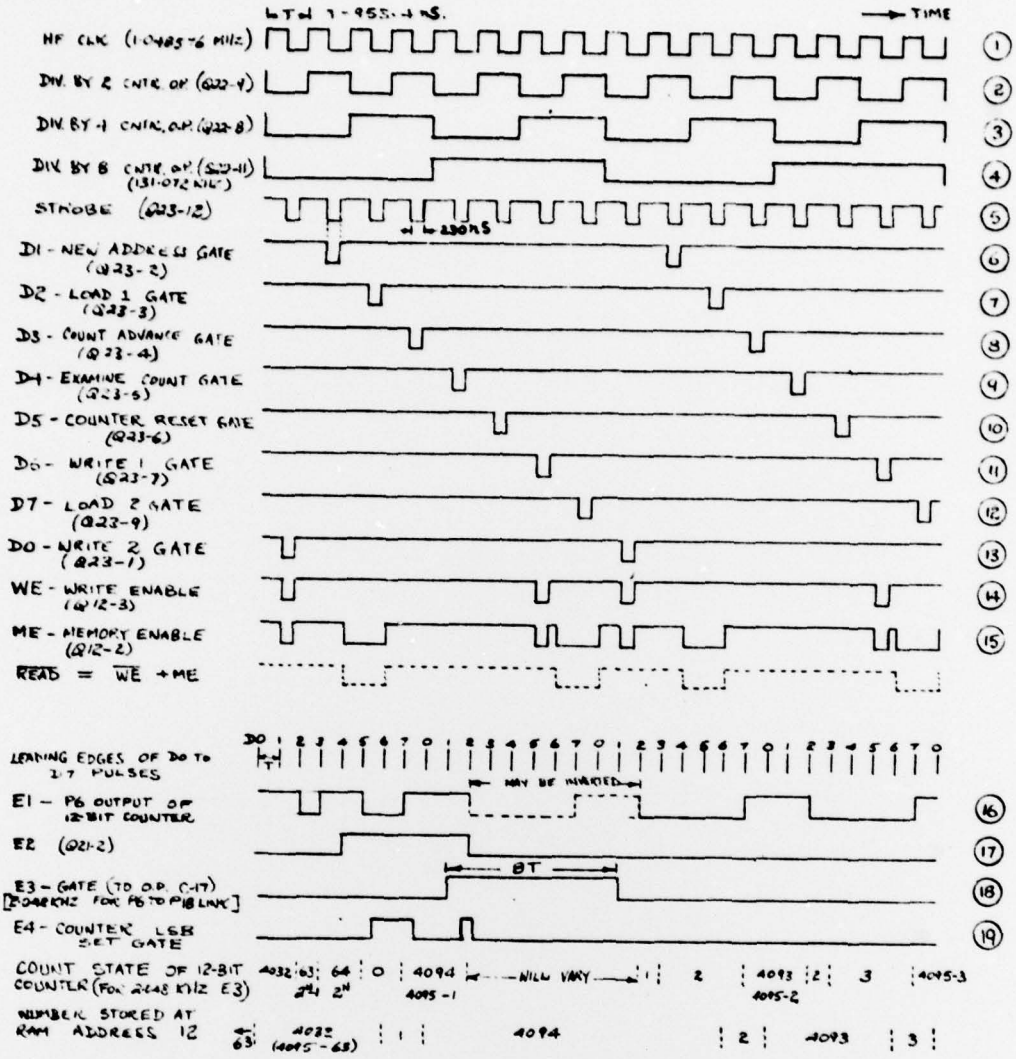


FIG. 9 WAVEFORMS 1 TO 19 FOR PRE-COUNTER

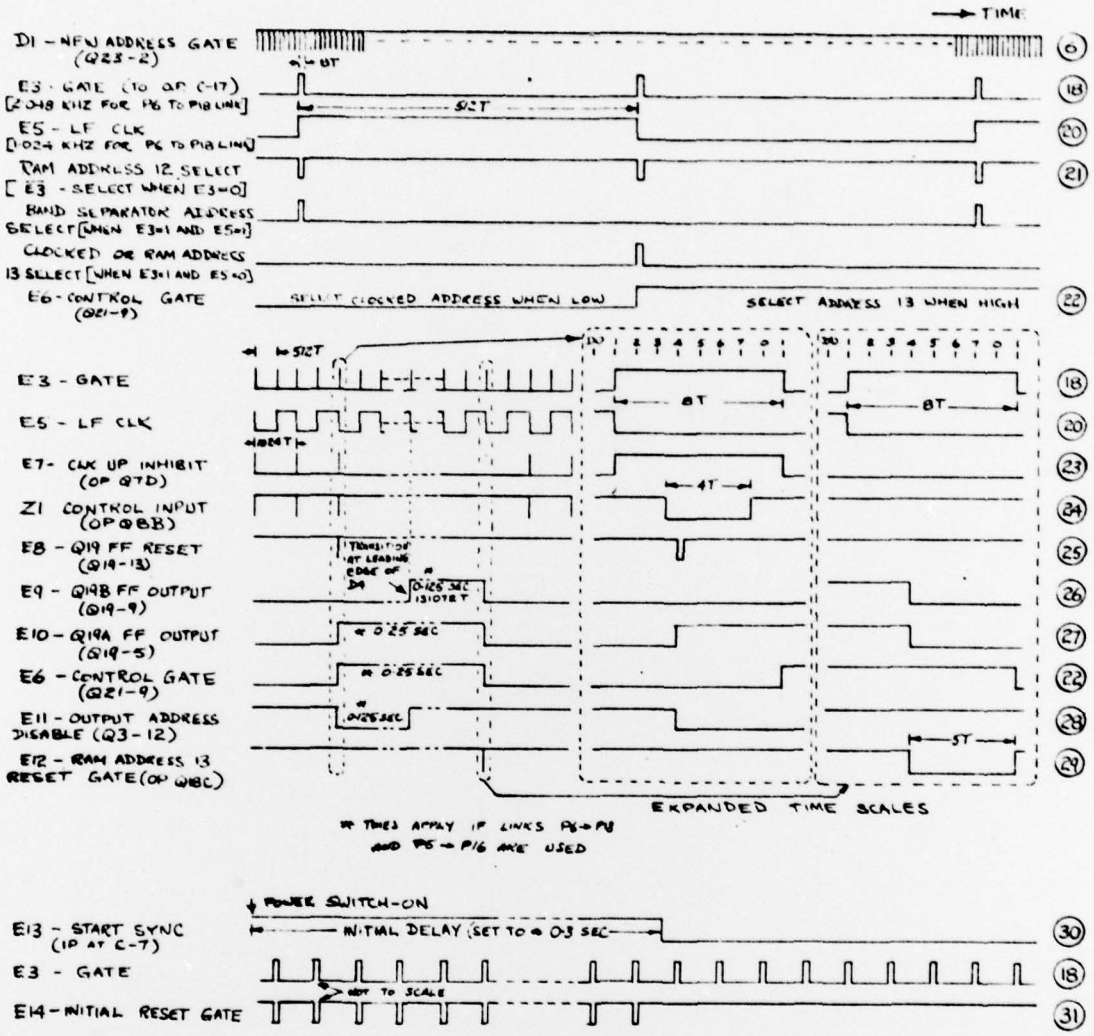


FIG. 10 WAVEFORMS 20 TO 31 FOR PRE-COUNTER

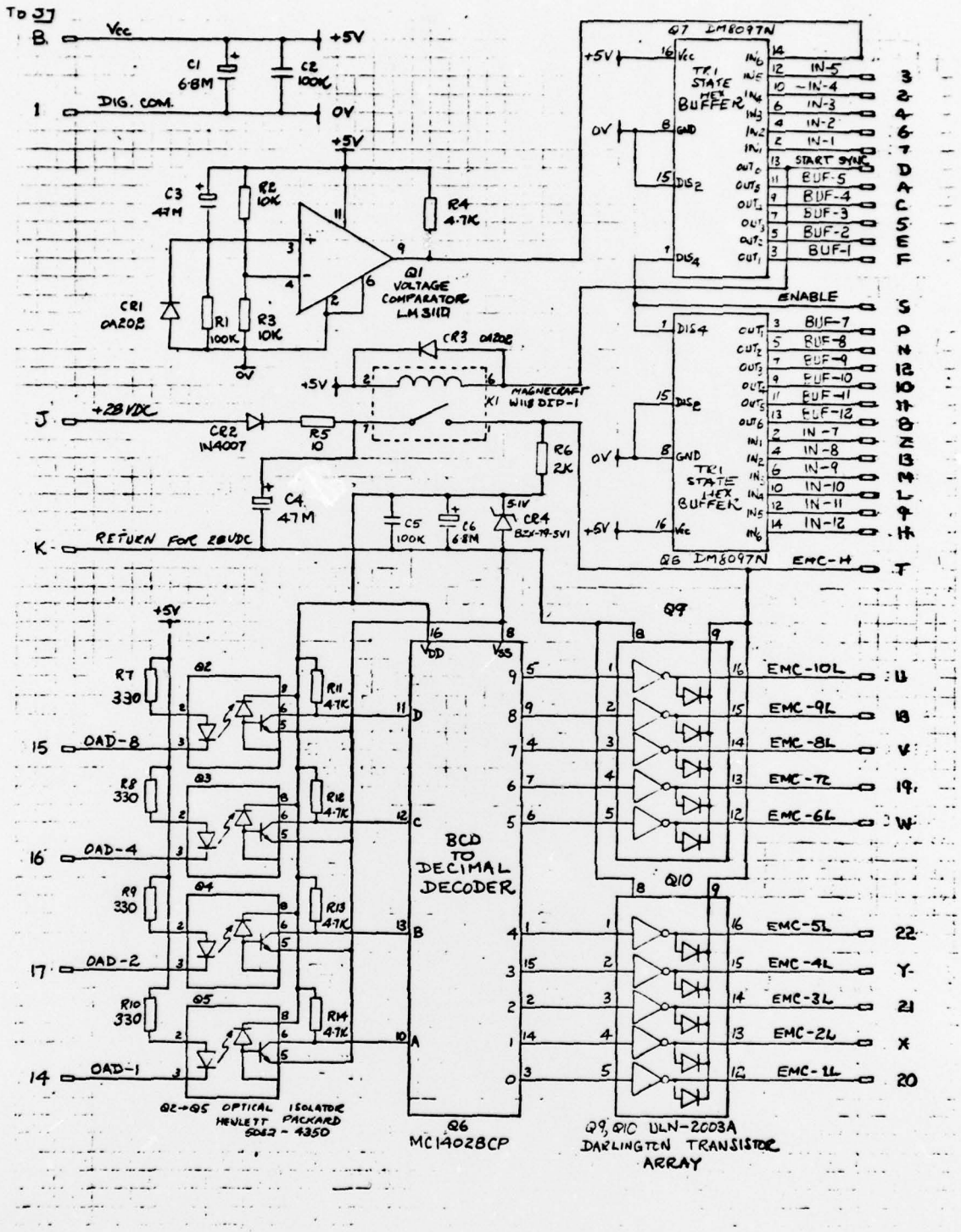


FIG. 11 START SYNC GENERATOR AND OUTPUT DRIVER CIRCUIT

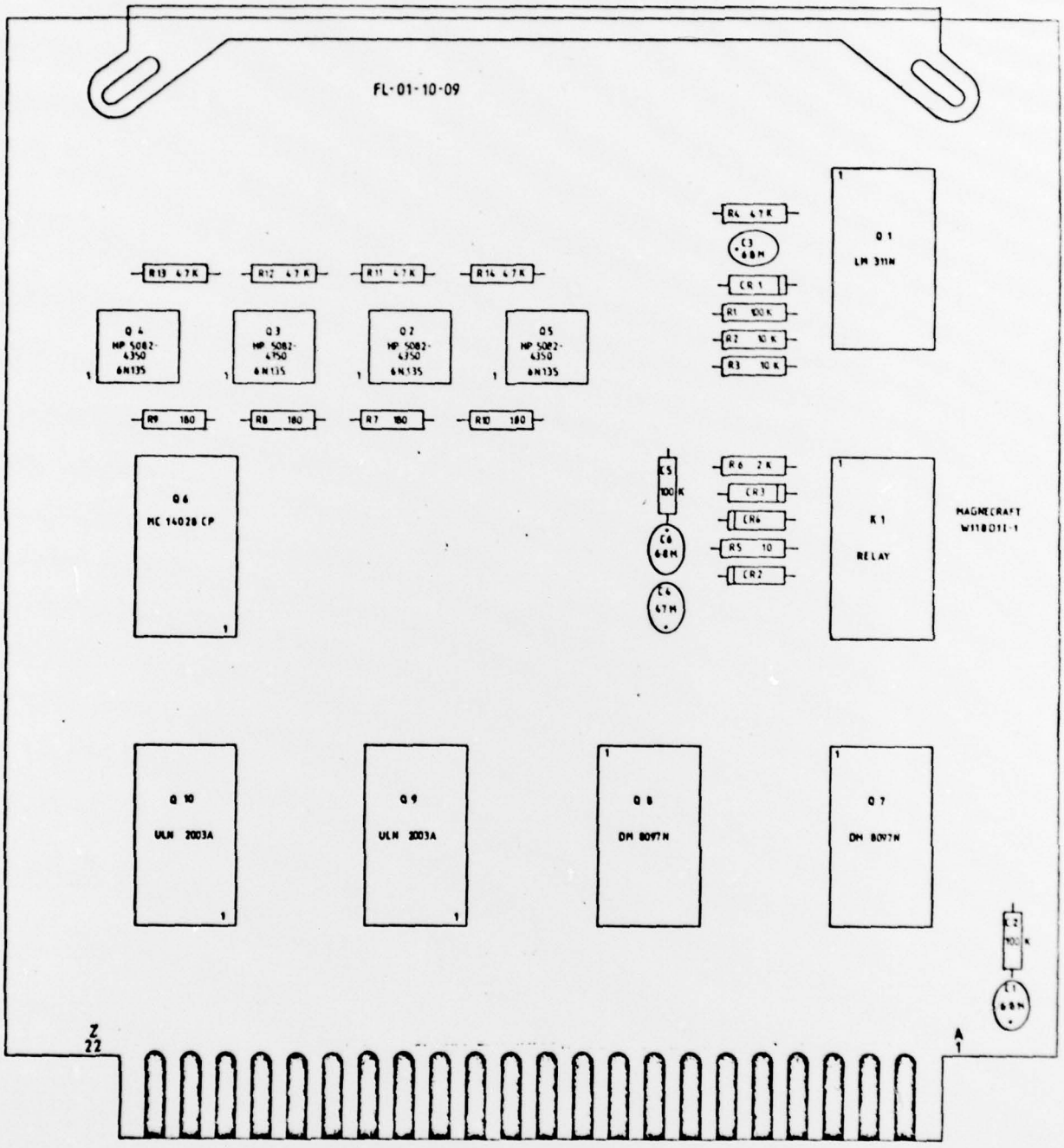


FIG. 12. COMPONENT LAYOUT FOR START SYNC GENERATOR AND OUTPUT DRIVER CIRCUIT

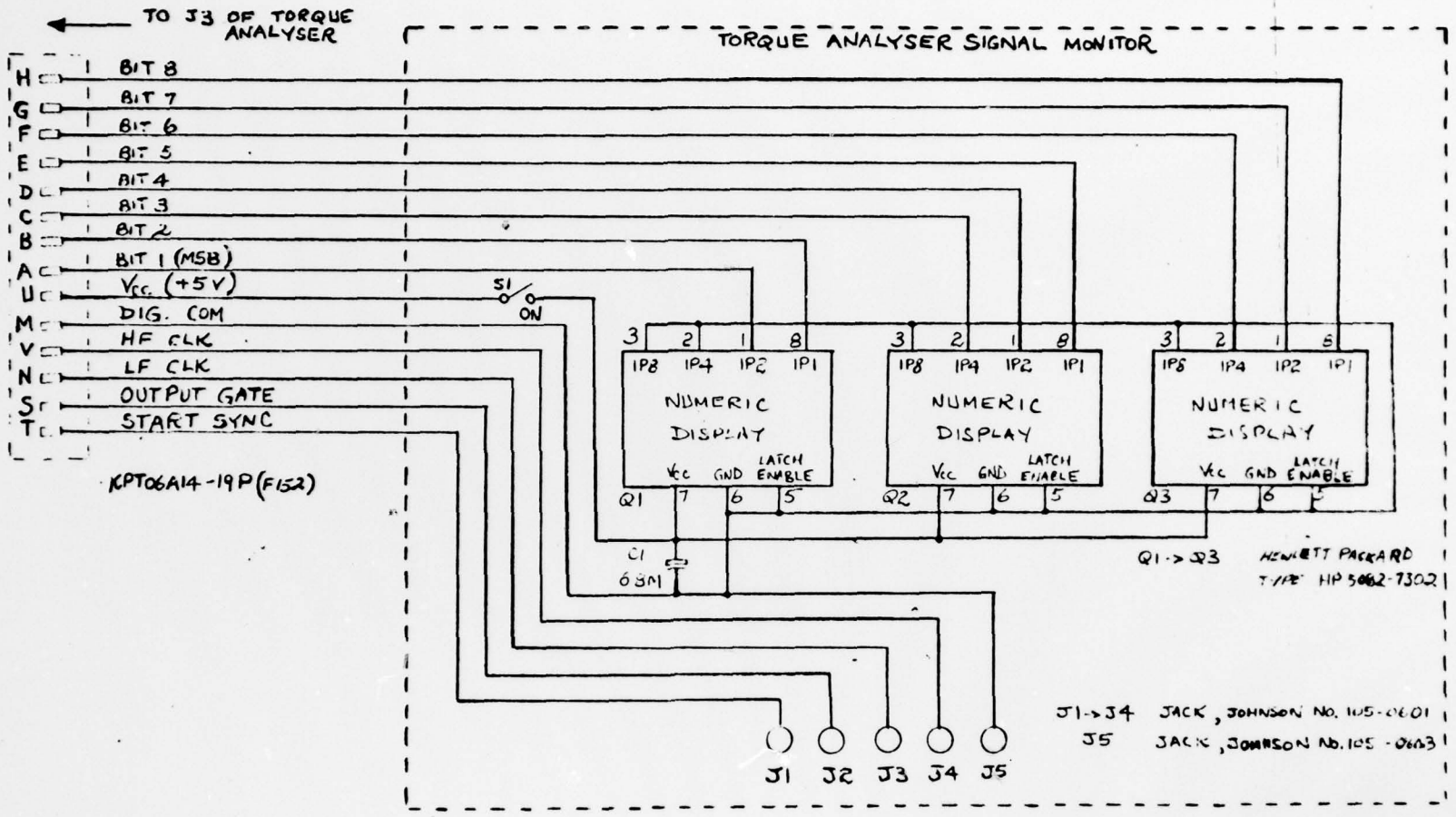


FIG. 13 TORQUE SPECTRUM INDICATOR SIGNAL MONITOR

FIG. 14 TORQUE SPECTRUM INDICATOR

DOCUMENT CONTROL DATA SHEET

Security classification of this page: Unclassified

1. Documents Numbers
   (a) AR Number:
   AR-001-303
   (b) Document Series and Number:
   Mechanical Engineering Note 372
   (c) Report Number:
   ARL-Mech-Eng-Note-372

2. Security Classification
   (a) Complete document:
   Unclassified
   (b) Title in isolation:
   Unclassified
   (c) Summary in isolation:
   Unclassified

3. Title: LOAD SPECTRUM MEASURING EQUIPMENT—PART 2

4. Personal Author(s):
   K. F. Fraser
   & U. R. Krieser

5. Document Date:
   September, 1978

6. Type of Report and Period Covered:

7. Corporate Author(s):

8. Reference Numbers
   (a) Task:
   NAV 76/248
   (b) Sponsoring Agency:
   DNAE

9. Cost Code:
   44 8875

10. Imprint:
    Aeronautical Research Laboratories,
    Melbourne

11. Computer Program(s)
    (Title(s) and language(s)):

12. Release Limitations (of the document)
    Approved for public release

12-0. Overseas:	No.		P.R.	1	A		B		C		D		E	

13. Announcement Limitations (of the information on this page):
    No limitation

14. Descriptors:

		15. Cosati Codes:
Loads (forces)	Transducers	0901
Torque	Electromechanical Transducers	1402
Automotive Transmissions	Analogue to Digital Converters	2011

15.

ABSTRACT

Measuring equipment which uses a set of electromechanical counters to indicate either the integrated time in seconds for which torque loading on a transmission component falls within each of a number of bands or the number of times each of a number of torque-bands is traversed, is described. Separation of the torque level into bands is made possible using a single transducer, an amplifier with zero and gain adjustments for setting the extremes of the torque range of interest, an analogue to digital converter and decoder to separate the torque range into bands and counters to totalize the contributions relevant to each band.

DISTRIBUTION

	Copy No.
AUSTRALIA	
DEPARTMENT OF DEFENCE	
Central Office	
Chief Defence Scientist	1
Executive Controller, ADSS	2
Superintendent, Defence Science Administration	3
Australian Defence Scientific and Technical Representative (UK)	4
Counsellor, Defence Science (USA)	5
Defence Library	6
JIO	7
Assistant Secretary, DISB	8–23
Aeronautical Research Laboratories	
Chief Superintendent	24
Superintendent—Mechanical Engineering Division	25
Divisional File—Mechanical Engineering Division	26
Authors: K. F. Fraser	27
U. R. Krieser	28
Library	29
F. W. Hooton	30
C. N. King	31
Materials Research Laboratories	
Library	32
Defence Research Centre	
Library	33
Central Studies Establishment Information Centre	
Library	34
Engineering Development Establishment	
Library	35
RAN Research Laboratory	
Library	36
Navy Office	
Director of Naval Aircraft Engineering, Canberra	37–39
Superintendent, Aircraft Maintenance and Repair, Sydney	40
OIC, Aircraft Maintenance and Flight Trials Unit—NAS, Nowra	41
Naval Scientific Adviser	42
Army Office	
Army Scientific Adviser	43
Air Office	
Air Force Scientific Adviser	44
Aircraft Research and Development Unit	45
Engineering, (CAFTS), Library	46
HQ Support Command, (SENGSO)	47

UNITED STATES OF AMERICA

NASA Scientific and Technical Information Facility	147
Cessna Aircraft Co. (Mr. D. W. Mallonee, Executive Engineer)	148
General Electric (Aircraft Engine Group)	149
Lockheed Aircraft Co. (Director)	150
McDonnell Douglas Corporation (Director)	151
United Technologies Corporation, Fluid Dynamics Laboratories	152
Spares	153–162